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Development and Research of Models and Processes of Formation in Silicon Plates p-n Junctions and Hidden Layers under the Influence of Ultrasonic Vibrations and Mechanical Stresses

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Abstract. In this article, mathematical models and processes of introducing homogeneous ultrasonic oscillations and mechanical stresses into silicon wafers in the direction of their thickness are developed and investigated, and mathematical models of the movement of interstitial defects in silicon wafers created by the processes of ion-beam transients at the transitions of ion-beam transitions and hidden dielectric layers using the action of ultrasound oscillations and mechanical stresses, both in the process of implantation of impurities and before the annealing of plates upon activation of the impurities are developed and investigated.

Introduction

Electronic engineering is at the forefront today’s important innovations. Now it contributes to modern changes in mobile technology, energy efficiency, transportation and control [1]. That is why researching characteristics of semiconductors is of a great interest.

Ion beam implantation of impurities *B*, *P*, *Sb*, *As* in semiconductor materials causes the destruction of the crystalline lattice of the surface layer, resulting in different kinds of defects: between nodal atoms, the absence of atoms at nodes (vacancies or Schottky defects), Frenkel defects, etc. [2]. In traditional methods of defect healing, heat treatment of semiconductor wafers (annealing) is carried out at temperatures 650-700 ºC. During annealing, thermal expansions increase the nodal distances, reduce energy barriers between the balanced states of atoms and defects, and intensify their thermal fluctuations. These processes activate the migration of defects and increase the likelihood of their approach to a critical distance at which defects of the type "vacancy" and "atom between nodes" are neutralized [3]. In general, the crystal lattice acquires a balanced state with a minimum number of defects.

Similar effects, namely the expansion of the crystal lattice and the intensification of vibrations of atoms and defects, can be obtained by the excitation of acoustic vibrations in semiconductor wafers. Appropriate methods for processing ion-implanted semiconductor wafers have been called ultrasonic treatment (in situ UST) [4].

According to the literature, ultrasonic treatment of ion-implanted semiconductor wafers contributes to the formation of high-quality p-n junctions (shallow distribution depth, distribution profiles close to rectangular, reduced back currents, etc.) compared to p-n junctions obtained by annealing [5]. Although, microelectonic devices are deeply researched and developed [6], available literature does not answer the questions about both the reasons for the improvement of the quality of p-n junctions obtained using ultrasonic processing (ultrasound p-n junctions) and the mechanisms of this phenomenon. But even a superficial comparison of the effects of thermal and ultrasonic treatments in terms of crystal lattice expansion and oscillation intensification is not in favor of ultrasound treatment (more on this below).

In this regard, there was a need for a theoretical justification for the experiment, which would allow a controlled ultrasonic treatment of ion-implanted semiconductor plates (such as silicon) and obtain reliable quantitative data both to elucidate the mechanism of influence of ultrasonic processing on the quality of p-n junctions, and lay the foundations for the development of appropriate technology for the manufacture of ultrasound p-n junctions. The main difficulties encountered in the ultrasonic processing of semiconductor wafers are related to the control of their intensity [7]. In this article a technique for controlling the intensity of acoustic oscillations is represented, which relies on determining the resulting figure of Q factor of a multilayer structure of a semiconductor-piezoelectric by the frequency response of the piezoelectric exciter current.

Purpose. Mathematical models of the processes of introduction of dynamic ultrasound oscillations and control of their intensity in ion-implanted silicon wafers by static clamping of them to a piezoelectric plate with subsequent excitation of high-frequency ultrasound oscillations in a multilayer structure of a semiconductor-piezoelectric by applied to the piezoelectric plate electrical voltage are developed.

The objects of research are the processes of introduction of ultrasound oscillations and mechanical stresses into silicon wafers and their influence on the displacement of interstitial defects created by ion-beam implantation of impurities during the formation of p-n junctions and hidden layers.

Methodology. Theoretical analysis of the processes of introduction of ultrasound oscillations and mechanical stresses into silicon wafers.

Justification of Semiconductor-Piezoelectric Structures and Basic Simplifications

The thickness of semiconductor silicon wafers in the manufacture of p-n junctions, as a rule, does not exceed 0.5 mm with a diameter of 100 mm [2]. In this ratio of dimensions, the effective excitation of acoustic oscillations of the proper intensity can be carried out by the wide surfaces (bases), providing acoustic contact between the semiconductor plate and the exciter, as it is advisable to use piezoelectric materials - piezoceramic or single crystalline plates, for example $LiNbO_3$.

Traditional methods of introducing acoustic oscillations into semiconductor wafers are used by matching fluid layers, which, first, pollute the technology and, second, non-technological for use in industrial production. Another way to ensure acoustic contact between the semiconductor plates and the exciter lies in the static compression of the plates, which can be carried out in the chamber with proper sealing of the multilayer structure of the semiconductor-piezoelectric perimeter. But in this case, the intensity of the dynamic acoustic vibrations caused by the itch cannot exceed the mechanical stresses of static compression. Therefore, the resulting mechanical stresses will be compression stresses, and the expansion of the crystal lattice will not be observed and it is likely that the healing of defects will slow down. The raised issues need further experimental study, since the mechanism of the influence of acoustic vibrations on the quality of ultrasound p-n junctions is not fully understood.

In Fig. 1 a symmetric five-layer semiconductor-piezoelectric structure is shown, where regions 1, 2, 3, 4 – are silicon plates, and region 0 – is a piezoelectric plate. If piezoelectricity is used for piezoelectric ceramics, the letter P with the arrow near it determines the polarization of the piezoelectric ceramics. When using single-crystal piezoelectrics, the letter P and the arrow determine one of the most piezoactive directions. For example, for single crystal piezoelectric $LiNbO_3$ the largest values among the longitudinal piezomodules are the piezomodules d_{22} i d_{33} [11]. Bold lines in Fig. 1 are marked electrodes that are deposited on the surface of a piezoelectric plate which thickness is considered neglected.

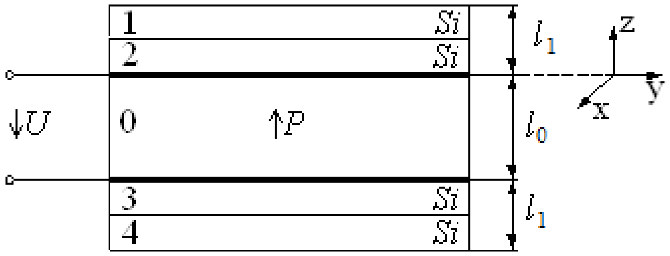

Fig. 1. Symmetrical five-layer structure of semiconductor-piezoelectric

The number of semiconductor plates may be greater than four, but the overall thickness of the multilayer structure $L = 2l_1 + l_0$ should be much smaller than the transverse dimensions (five to ten times) and in the analysis of thickness fluctuations the whole multilayer structure can be considered a "wide and thin" plate [8].

Fastening and sealing elements in fig. 1 are not indicated, but are considered to be located along the perimeter at a distance from the edge of not more than the total thickness of the multilayer structure. Under these conditions, in accordance with the Saint-Wenack principle [7], the influence of the fastening and sealing elements on the oscillation thickness will be manifested at a distance from the edge of not more than double the thickness of the multilayer structure. Therefore, the main area of the broad surfaces of the structure of fig. 1 in the analysis of dynamic thickness fluctuations can be considered free from dynamic mechanical stresses. The fastening and sealing elements will influence to some extent the resultant figure of Q factor, which should be measured experimentally.

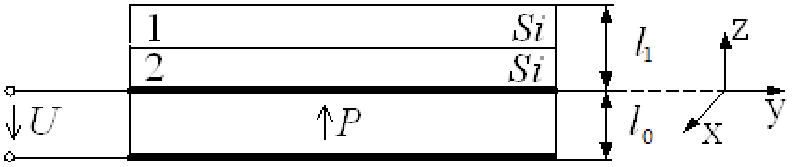

Fig. 2. Asymmetric three-layer structure of semiconductor-piezoelectric

In Fig. 2 an alternative asymmetrical three-layer structure is shown, to the dimensions and elements of fastening and sealing of which are subject the same requirements as to the symmetrical structure.

The boundaries of the interlayer section are considered to be infinitesimal and their effect on the oscillation thickness neglected. In addition, since the acoustic resistance does not change at the interface boundaries of semiconductor wafers, the set of contacting semiconductor wafers is considered as one plate (one layer).

Equivalent Schemes of Multilayer Structures

Wide and thin plate of the equivalent scheme. The description of the thickness fluctuations in multilayer structures can be carried out both by using differential equations and by equivalent schemes of individual layers. The last option is more common in engineering practice, so let's dwell on it.

In Fig. 3 an equivalent scheme of a "wide and thin" piezoelectric plate for the excitation of thickness oscillations is shown [8], where F_1 and F_2 – mechanical forces that are applied to wide surfaces, U and I is the voltage between the electrodes and the current through the piezoelectric plate, n is the transformation ratio of the ideal transformer.

Equivalent circuits of semiconductor layers are obtained from the scheme in Fig. 3 if $n = 0$ is accepted.

The parameters of equivalent circuits will be defined below for each structure, after their transformation, per unit area of a wide surface.

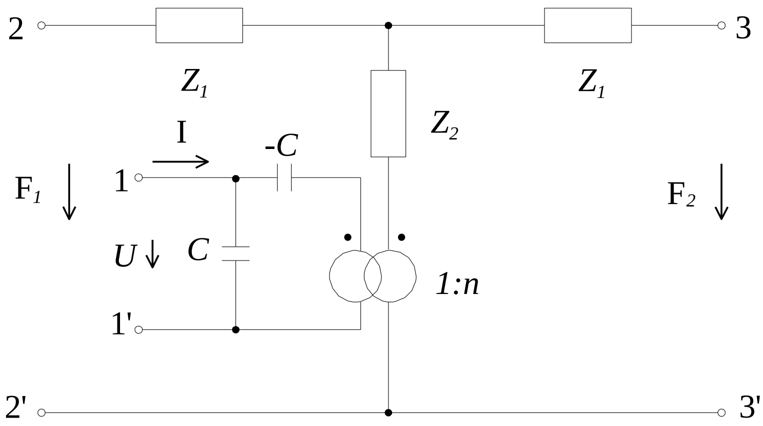

Fig. 3. Equivalent scheme of the "wide and thin" piezoelectric plate

The poles 2-2' and 3-3' correspond to wide surfaces and if the surface is vacant then the corresponding poles should be shortened. If the wide surface is in contact with the surface of the other plate, the respective poles of the two plates are joined.

Symmetrical structure. The symmetrical structure, irrespective of the number of silicon wafers, consists of three homogeneous layers and its equivalent scheme is obtained by connecting three equivalent circuits of the form in Fig. 3, the outer poles corresponding to the free surfaces should be shortened. The corresponding equivalent scheme of the three-layer structure, taking into account the symmetry, is transformed to the appearance on Fig. 4,

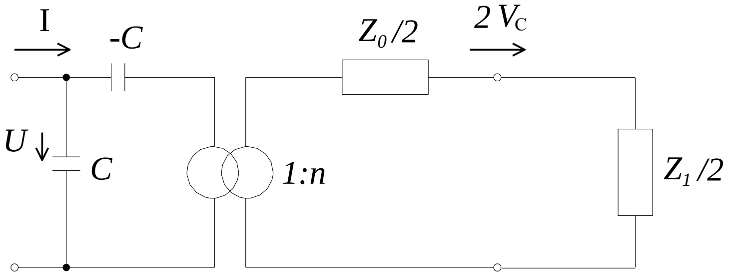

Fig. 4. The transformed equivalent scheme of the symmetric multilayer structure

where $C = \frac{\varepsilon^S}{l_0}$ is specific electrical input capacity of the piezoelectric plate (ε^S is the dielectric constant of the clamped plate);

$$n = g_{33} C_{33} \varepsilon^S \frac{1}{l_0}, \tag{1}$$

- transformation factor of the perfect transformer that converts electrical voltage and current into mechanical power and speed (g_{33} is the piezomodule, C_{33} is Young's module [6]);

$$Z_0 = -jV_0 \rho_0 ctg \frac{\omega l_0}{2V_0}, \tag{2}$$

- specific equivalent resistance of piezoelectric plate at thickness fluctuations ($V_0 = \sqrt{\frac{C_{33}}{\rho_0}}$ is the speed of acoustic waves, ρ_0 is density of piezomaterial, ω is angular excitation frequency, j is the imaginary unit);

$$Z_1 = jV_1 \rho_1 tg \frac{\omega l_1}{V_1}, \tag{3}$$

- specific equivalent resistance of silicon wafers ($V_1 = \sqrt{\frac{C'_{33}}{\rho_1}}$ is the speed of acoustic waves in silicon; C'_{33} is Young's module, ρ_1 is density); V_C is the speed of movement of the boundary of the semiconductor-piezoelectric section of symmetric structure.

Asymmetrical structure. An equivalent scheme of an asymmetric structure is formed by the conjunction of two equivalent circuits of the form in Fig. 3 with shortened outer poles, which after transformations takes the form in Fig. 5,

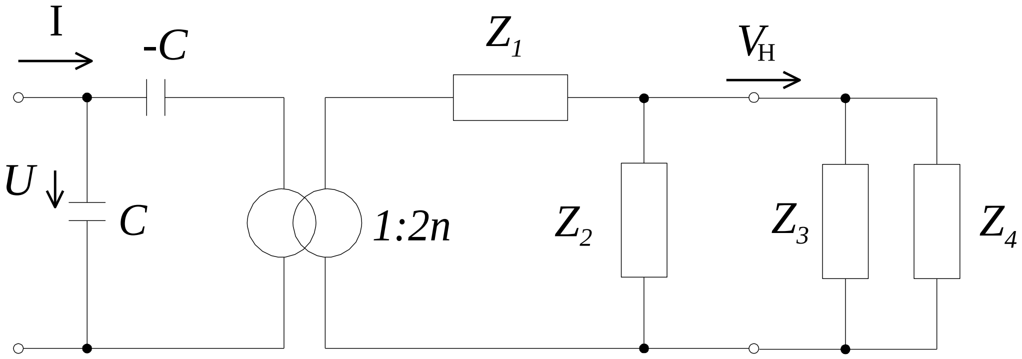

Fig. 5. The transformed equivalent scheme of the symmetric multilayer structure

in which the parameters C and n coincide with the parameters of the symmetric structure and the other parameters are determined by the formulas

$$Z_1 = -j2\rho_0 V_0 ctg \frac{\omega l_0}{2V_0}, \tag{4}$$

$$Z_2 = j2\rho_0 V_0 tg \frac{\omega l_0}{2V_0}, \tag{5}$$

$$Z_3 = j2\rho_1 V_1 tg \frac{\omega l_1}{2V_1}, \tag{6}$$

$$Z_4 = -j2\rho_1 V_1 ctg \frac{\omega l_1}{V_1}, \tag{7}$$

where ρ_0, V_0, ρ_1, V_1 also match the corresponding symmetric structure parameters; V_H is the velocity of displacement of the asymmetric structure semiconductor-piezoelectric interface.

Analysis of Symmetric Multilayer Structure

Determination of strain distribution over the thickness of a semiconductor. The intensity of acoustic oscillations in silicon wafers is determined by the speed of movement of their surface, which contacts the surface of the piezoelectric. According to the scheme in Fig. 4 we find the velocity of the interface boundary for a symmetric structure

$$V_C = \frac{nU}{j\left[V_1\rho_1 tg\beta_1 l_1 + V_0\rho_0\left(\frac{2k_t^2}{\beta_0 l_0} - ctg\frac{\beta_0 l_0}{2}\right)\right]}, \tag{8}$$

where k_t is the electromechanical coupling coefficient, $\beta_1 = \frac{\omega}{V_1} = \frac{2\pi}{\lambda_1}$ and $\beta_0 = \frac{\omega}{V_0} = \frac{2\pi}{\lambda_0}$ are constant propagation of acoustic waves in semiconductor and piezoelectric, λ_1 and λ_0 are corresponding wavelengths [8].

Given the known velocity of one surface of the plate and the condition that the opposite surface is free, we find the velocity of movement of material particles in a semiconductor with an arbitrary coordinate *Z* (the coordinate *Z* is deduced from the interface of the semiconductor and piezoelectric) [10].

$$\xi = \frac{V_C}{\cos \frac{\omega}{V_1} l_1} \cos \frac{\omega}{V_1} \left(Z - l_1 \right). \tag{9}$$

Next, we find the distribution of deformation in the silicon wafer

$$S = \frac{d\xi}{dZ} = g_{33} \varepsilon_{33}^{S} \frac{V_0}{V_1} \frac{U}{l_0} f_C(\omega) \left(\sin \beta_1 Z - tg \beta_1 l_1 \cos \beta_1 Z \right), \tag{10}$$

where $f_C(\omega)$ is the frequency function of symmetric structure, which is determined by the expression

$$f_C(\omega) = \frac{1}{\frac{\rho_1 V_1}{\rho_0 V_0} tg \beta_1 l_1 - ctg \frac{\beta_0 l_0}{2} + 2 \frac{k_t^2}{\beta_0 l_0}}. \tag{11}$$

By decomposing the frequency function into a simple fraction and considering the energy losses, we obtain the distribution of the strain amplitude over the thickness of the semiconductor wafers that excited by the resonance modes of the thickness oscillations [8]

$$S_n = g_{33} \varepsilon_{33}^{S} \frac{V_0}{V_1} \frac{U_m}{l_0} B_n Q_n \left(\sin \beta_1 Z - tg \beta_1 l_1 \cos \beta_1 Z \right), \tag{12}$$

where Q_n is the resultant Q-factor of a multilayer structure in the *n*-th resonance mode (*n* is an integer multiple of the number of half waves embedded in the piezoelectric thickness and assuming 1, 3, 5,…).

Coefficient B_n in the *n*-th pole of the frequency function is determined by the expression:

$$\mathrm{B}_n = \frac{2x_n^{-1}}{m \frac{\pi}{x_n} \frac{\rho_1 V_1}{\rho_0 V_0} \cos^{-2} k x_n + \sin^{-2} x_n - k_t^2 x_n^{-2}}, \tag{13}$$

where x_n is the *n*-th root of the frequency equation

$$\frac{\rho_1 V_1}{\rho_0 V_0} tg k x_n - ctg x_n + \frac{k_t^2}{x_n} = 0, \tag{14}$$

the left part of which coincides with the denominator of the frequency function when replacing $x = \frac{\omega l_0}{2V_0}$, $k = \frac{2V_0 l_1}{V_1 l_0}$, and m is the number of half-waves in the silicon wafer $\left(m = \frac{2l_1}{\lambda_1} \right)$.

If the total thickness of the silicon wafers at the frequencies of resonant oscillations is a multiple of the half-wavelength, ie $l_1 = \frac{m\lambda_1}{2}$, then $kx_n = m\pi$, and $tgkx_n = 0$. In this case, the frequency equation is simplified and takes the form

$$xctgx - k_t^2 = 0, \tag{15}$$

and coefficient expressions B_n

$$B_n = \frac{2x_n}{m\pi x_n \left(\frac{\rho_1 V_1}{\rho_0 V_0} + x_n^2 - k_t^2 \left(1 - k_t^2 \right) \right)}, \tag{16}$$

and distribution of the amplitude of the deformation along the thickness of the semiconductor in the *n*-th resonant mode

$$S_n \approx d_{33} \left(1 - k_t^2 \right) \frac{V_0}{V_1} \frac{U_m}{l_0} B_n Q_n \sin n\pi \frac{Z}{l_1}, \tag{17}$$

where $d_{33} = \frac{g_{33} \varepsilon_{33}^S}{\left(1 - k_t^2 \right)}$ is the piezomodule [6].

At the roots of the frequency equation, the piezoelectric thickness required for the resonant mode to occur at frequency ω_n, is calculated by the expression $l_0 = 2\frac{x_n V_0}{\omega_n}$. Moreover, at $n = 1$ the piezoelectricity is embedded in a half-wave, *n* = 3 – one and a half waves, *n* = 5-2.5 waves, etc. The frequencies at which the piezoelectricity is embedded in an even number of half-waves are not excited. The total thickness of the semiconductor layers should be chosen so that the integer number of half-waves is enclosed. The corresponding thickness is calculated by the expression

$$l_1 = m \frac{\pi V_1}{\omega_n} = m \frac{\pi V_1 l_0}{2 x_n V_0}, \tag{18}$$

where ω_n - *n*-th resonant excitation frequency.

The maximum deformation amplitude occurs when the fundamental resonant mode is excited (*n* = *m* = 1) and is observed in the middle of the semiconductor plate $\left(Z = \frac{l_1}{2} \right)$ and decreases to zero at the edges.

Estimation of the Maximum Deformation of a Semiconductor

To estimate the maximum deformation, we must find the roots of the frequency equation. The solution of the simplified frequency equation (15) for $k_t^2 = 0.25$ gives the following three roots: $x_1 = 1.3932$; $x_3 = 4.6588$; $x_5 = 7.8220$. Subsequent root values asymptotically approach the values $x_n = \frac{n\pi}{2}$, *n* = 7, 9, 11, …, remaining less than it.

In which modes of frequency oscillation acoustic stimulation of ion-implanted semiconductor *p-n* junctions will be most effective to determine the experiment. This mode is likely to be the lowest ($n = 1$, $m = 1$). For this case, in Tab. 1 the data of the lowest root of the frequency equation (15) the data of the lowest root of the frequency equation (15) x_1 and coefficient B_{1C} (symmetric structure) for materials semiconductor (silicon) are shown: $\rho_1 = 2328$ kg/m^3, $V_1 = 9850$ m/s; piezoelectric (LiNbO$_3$): $\rho_0 = 4630$ kg/m^3, $V_0 = 7200$ m/s (semiconductor and piezoelectric thicknesses are half-wave: $n = m = 1$) [11].

Table 1. The dependence of the roots of the frequency equation and coefficients B_{1C} symmetrical and B_{1H} asymmetric structures from the coefficient of electromechanical coupling

k_t^2	0.25	0.2	0.15	0.1	0.05
x_1	1.3932	1.4320	1.4690	1.5044	1.5383
B_{1C}	0.5848	0.5745	0.5644	0.5547	0.5452
B_{1H}	0.8622	0.8330	0.8121	0.7920	0.7728

Note. In the fourth line of the table 1 the coefficient B_{1H} for the asymmetric structure is shown.

With decreasing electromechanical coupling coefficient, the smallest root of the frequency equation approaches the value of $x_1 = \frac{\pi}{2} \approx 1.5708$.

Numerical estimation of maximum deformation will be carried out for a three-layer structure of a semiconductor (*Si*) - piezoelectric (*LiNbO*$_3$), when each layer is half-wave.

Additional *LiNbO*$_3$ parameters: piezomodule $d_{33}=19\cdot10^{-12}$ Cl/N; $k_t^2= 0.1936\approx0.2$ [11].

According to the formula (17), the known material parameters and the data of the Table 1 (for $n = 1$ and $Z = l_1/2$), we find

$$S_1 \approx 6.0\, Q_1 \frac{U_m}{l_0}, \tag{19}$$

where the voltage amplitude U_m is taken in volts, and the piezoelectric thickness l_0 in meters. The ratio $\frac{U_m}{l_0} = E_{m0}$ determines the amplitude value of the electric field strength in the piezoelectric, which should not exceed the breakdown, and the coefficient 6.0 of Q_1 shows how in a symmetric structure the electric field strength in the piezoelectric transforms into a semiconductor deformation.

The relation (19) actually allows to control the intensity of acoustic vibrations in semiconductor wafers, if the value of Q-factor of the multilayer structure is known.

Let us estimate the possible values of the structure factor on the basis of the data on the attenuation of waves in silicon and *LiNbO*$_3$.

According to the guide [11] in the GHz range the attenuation coefficients of the waves in silicon (α_1) and *LiNbO*$_3$ (α_0) (depending on the direction of propagation) are in the range $\alpha_1 = (5.9\text{-}7.6)$ dB/cm (with an error not exceeding 10%); $\alpha_0 = 0.34$ dB/cm (data on scatter values and error are missing).

The corresponding values of the value of Q-factor of the materials are calculated by the expression $Q = \frac{\pi}{\alpha\lambda}$ [8], where λ - wavelength in meters, and α - attenuation factor in Np/m. Assuming that the wave attenuation coefficients in *Si* and *LiNbO*$_3$ at the lowest resonant mode of the thickness oscillations keep the same values as at frequency 1 GHz, then the values of Q-factors of *Si* (Q_1) and *LiNbO*$_3$ (Q_0) will be: Q_1 = 46-36, Q_0 = 1100. It follows that the Q-factor of the multilayer structure will be determined by silicon. But the resulting value of Q-factor of the multilayer structure will be lower than the mechanical value of Q-factor of *Si*, since there are still structural energy losses caused by the attachment and sealing of the structure, and losses at the boundaries of the semiconductor-piezoelectric section. It is almost impossible to carry out a theoretical assessment of the resulting value of Q-factor of a structure and it will have to be measured experimentally.

Taking on the resulting value of Q-factor $Q = 30$, and E_{m0}=100 V/mm, we obtain the strain amplitude $S_1 = 1.8 \cdot 10^{-5}$. Compare the deformation value obtained below with the maximum allowable for silicon.

According to the guide [11], the mechanical compressive strength of silicon is $9{,}55 \cdot 10^{7}$ N/m^2, and the modulus of elasticity for the compression-tensile deformation is approximately $1{,}65 \cdot 10^{11}$ N/m^2. Based on this data, according to Hooke's law, we find the maximum allowable compression strain $S_{\mathrm{m.d.}} \approx 5.8 \cdot 10^{-4}$, which is 32 times larger than the value $S_1 = 1.8 \cdot 10^{-5}$, obtained from the calculations.

There are no data on the mechanical tensile strength of silicon, but it is to be expected that this tensile strength will be lower than that of compression.

Let us also estimate what the electric field strength should be in $LiNbO_3$, so that the dynamic deformation in silicon during acoustic excitation equals the maximum allowable $S_{m.d.}$. It is clear from previous estimates that such tensions will increase in 32 times and will be $E_{\mathrm{m.d.}} = 3200$ V/mm, which may exceed the electrical strength $LiNbO_3$ for dynamic mode (no data on the electrical strength $LiNbO_3$ are available).

Estimation of Piezoelectric Plate Thickness and Resonance Oscillation Frequency

The thickness of the silicon wafers generally does not exceed 0.5 mm [1] and, if such thickness is half-wave, then the wavelength in silicon λ_1= 1 mm. At the speed of acoustic waves in silicon V_1 = 9850 m/s [9] the lowest resonant frequency f_1 = 9,85 MHz.

The appropriate thickness of the piezoelectric plate of the material $LiNbO_3$, which must also be half-wave, at an acoustic wave velocity V_0 = 7200 m/s [9] will be (k_t^2=0.2)

$$l_0 = \frac{x_1 V_0}{\pi f_1} = \frac{2 l_1 x_1 V_0}{\pi V_1} \approx 0.33 \text{ mm.}$$

Perhaps that such a thickness of a single-crystal $LiNbO_3$ plate at a diameter of 100 mm will be almost unrealistic for manufacturing.

At the maximum allowable intensity of the excitation piezoelectric plate $LiNbO_3$ field $E_{m.d.}$ = 3200 V/mm, the maximum permissible amplitude of the exciting harmonic voltage should be $U_{m.d.} = E_{m.d} \cdot l_0 \approx 1000$ V, at the frequency f = 9.85 MHz.

It is clear that the excitation is not necessarily required to be based on the maximum permissible deformations of the silicon wafers or some other semiconductor. The determination of the optimal excitation mode, at which the quality of *p-n* junctions will be the best, should be investigated, since the mechanism of the influence of acoustic stimulation of ion-implanted semiconductors on the quality of *p-n* junctions, as already emphasized, has not been fully understood.

In order to reduce the excitation frequency and the corresponding increase in the thickness of the piezoelectric plate, it is necessary to increase the number of silicon wafers, leaving their total half-wave thickness. With the number of silicon wafers $2k$ (on k wafers at the top and bottom in symmetrical structure), the lowest resonant frequency will decrease and the thickness of the piezoelectric wafers will increase in k times.

But it should be borne in mind that the diameter of the multilayer structure is determined by the plates of silicon and is 100 mm, and the results of the analysis are made for the structure, which should be "wide and thin" plate. The condition of the same "wide and thin" plate is preserved if the total thickness of the structure is at least 5 times smaller than its diameter and does not exceed

20 mm [7]. Therefore, the total number of silicon wafers, taking into account the thickness of the piezoelectric plate cannot exceed 30 (l_1 = 7.5 mm), and the thickness of the piezoelectric plate is 5 mm.

With an aggregate thickness of 20 mm multilayer structure, the lowest resonant frequency will decrease to approximately 0.66 MHz, provided that the piezoelectric and silicon plates (top and bottom) are half-wavelength.

It should also be noted that during ion implantation of semiconductors, the surface layers in which the *p-n* junction is formed, are destroyed. Therefore, the maximum intensity of deformation should fall on the surface layers. It follows that the symmetrical and asymmetrical multilayered structure in Fig. 1 and Fig. 2 from below and from above should be covered with "ballast" layers of materials with high acoustic resistance (larger than silicon).

We can assume that more effective will be acoustic stimulation, the frequency of oscillations in which will vary within certain limits, around the frequency of half-wave resonance ($l_1 = \frac{\lambda_1}{2}$, $l_0 = \frac{\lambda_0}{2}$).

Analysis of Asymmetric Multilayer Structure

According to the scheme in Fig. 5 we find the velocity of displacement of the interface between a semiconductor and a piezoelectric asymmetric structure by the excitation of the thickness vibrations by the harmonic voltage

$$V_H = \frac{nU tg\frac{\beta_0 l_0}{2} tg\beta_0 l_0}{j\left[\rho_1 V_1 tg\beta_1 l_1\left(\frac{k_t^2}{\beta_0 l_0} tg\beta_0 l_0 - 1\right) + \rho_0 V_0 tg\beta_0 l_0\left(\frac{2k_t^2}{\beta_0 l_0} tg\frac{\beta_0 l_0}{2} - 1\right)\right]}, \tag{20}$$

where $\beta_1 = \frac{\omega}{V_1}$, $\beta_0 = \frac{\omega}{V_0}$ are continuous wave propagation in semiconductor and piezoelectric. Further, as for the symmetric structure, we first find the distribution of velocities of the material particles along the thickness of the semiconductor wafer by the formula (9) and then the distribution of the strain amplitude

$$S = d_{33}\left(1-k_t^2\right)\frac{V_0 U_m}{V_1 l_0} f_H(\omega)\left(\sin\beta_1 Z - tg\beta_1 l_1 \cos\beta_1 Z\right), \tag{21}$$

where the *Z* coordinate is also deduced from the boundary of the semiconductor and piezoelectric section.

The frequency function of an asymmetric structure $f_H(\omega)$ is determined by the expression

$$f_H(\omega) = \frac{tg\frac{\beta_0 l_0}{2} tg\beta_0 l_0}{\frac{\rho_1 V_1}{\rho_0 V_0} tg\beta_1 l_1\left(\frac{k_t^2}{\beta_0 l_0} tg\beta_0 l_0 - 1\right) + tg\beta_0 l_0\left(\frac{2k_t^2}{\beta_0 l_0} tg\frac{\beta_0 l_0}{2} - 1\right)}, \tag{22}$$

in which the quantities $\rho_1 V_1$, $\rho_0 V_0$ have the same meaning as for the symmetrical structure.

Similarly to the symmetric structure, decomposing the frequency function into a simple fraction and imposing the condition that the thickness of the semiconductor plate is a multiple of the half-wavelength ($l_1 = m\lambda_1/2$, m = 1, 2, 3) and taking into account the energy losses, we obtain the distribution of the strain amplitude over the thickness of *n*-th resonant mode defined by expression (17), where

$$B_n = \frac{2x_n}{\frac{m\pi x_n}{2}\cdot\frac{\rho_1 V_1}{\rho_0 V_0} + x_n^2 - k_t^2\left(1 - k_t^2\right)}. \tag{23}$$

The value of x_n is the root of the frequency equation (15), in which, as for a symmetric structure, it is accepted $x = \frac{\omega l_0}{2V_0}$. In the fourth line of the Tab. 1 the results of the calculation of the factor B_{1H} ($n = 1$, $m = 1$) for the asymmetrical structure, for the same values of the coefficient of electromechanical coupling, are shown.

Comparing the coefficients B_{1C} and B_{1H} (see Tab. 1), it follows that the efficiency of converting the electrical excitation voltage of the piezoelectric plate into mechanical deformation of the semiconductor in the asymmetric structure increased by about 30%. However, the quality factor of an asymmetric structure, provided that it is determined by the material quality of the semiconductor material, should also be higher.

The numerical estimates of the strain amplitude obtained for the symmetric structure are also preserved for the asymmetric one with the corresponding correction associated with the increase of the coefficient B_{1H}.

The choice of symmetric or asymmetric structures for acoustic stimulation of ion-implanted semiconductors depends, first of all, on their manufacturability, namely the conditions of attachment and sealing.

Comparison of the Effect of Thermal and Ultrasonic Treatments on the Processes in Silicon Wafers

During annealing, which occurs at temperatures of 650-700 ºC, there is a thermal expansion of the semiconductor and the accumulation of thermal energy in its volume. Acoustic oscillations cause similar effects: mechanical stresses are accompanied by compression-expansion deformations, and acoustic energy accumulates in the semiconductor volume. It is for these two consequences that we will compare the thermal and acoustic effects.

The specific heat of silicon at annealing temperatures is $C_p = 0.88\cdot 10^3$ J/kg·deg [11]. The increase in the density of the internal thermal energy of silicon during annealing will be $\Delta Q = C_p (T - T_0)$. If $T_0 = 20\ ^0C$, and T=650 ^{0}C, then $\Delta Q \approx 5.5\cdot 10^5$ J/kg. The maximum permissible bulk density of elastic energy for homogeneous deformation $W_m = \frac{1}{2} s T_m^2$, where s – compliance, and T_m – the maximum allowable mechanical stress, which for compression silicon is $9.55\cdot 10^7$ H/m^2 [9]. When compliant $s = 8\cdot 10^{-12}$ m^2/H [9] the maximum permissible bulk density of elastic energy $W_m = 3.6\cdot 10^4$ J/m^3. At silicon density $\rho = 2328.3$ kg/m^3, the density of elastic energy in terms of 1 kg will be approximately 16 J/kg, which is four orders of magnitude less than the density of thermal energy.

The coefficient of thermal expansion of silicon is determined by the expression [9]

$$\alpha_T = 3.0024\cdot 10^{-6} + 0.1544\cdot 10^{-8} T + 0.20576\cdot 10^{-11} T^2,$$

where temperature T is taken in ºK. At annealing temperature T = 650 ºC, the coefficient of thermal expansion $\alpha_{923} = 1.425\cdot 10^{-6}$ K^{-1}, and the temperature expansion $\Delta l / l \approx 1.3\cdot 10^{-3}$. The maximum allowable deformation of silicon during compression is $S_m = 5.8\cdot 10^{-4}$ that it is approximately twice less than the thermal expansion upon annealing.

The comparison of the effects of thermal and acoustic effects on the processes in silicon shows greater efficiency of thermal action. It can be assumed that the thermal action will more effectively affect the processes of "healing" of defects caused by the implantation of impurities. Therefore, in our opinion, the combination of thermal and acoustic action may be more effective than the action of each of them separately. The necessary heating of the silicon wafers may occur due to the loss of acoustic vibrations.

Experimental Determination of the Intensity of Acoustic Vibrations of Semiconductor Wafers

The strain amplitude distribution over the thickness of semiconductor wafers of symmetric and asymmetric structures in the nth resonance mode, provided that the thickness of semiconductor and piezoelectric layers is a multiple of the half-wave thickness ($l_1 = \frac{m\lambda_1}{2}$, $l_0 = \frac{\lambda_0 x_n}{\pi}$) is determined by expression (17), where d_{33}, k_t, V_0, V_1 are piezoelectric and semiconductors parameters that are known. The coefficients of symmetric and asymmetric structures are determined by formulas (16), (23) and also depend on the piezoelectric, semiconductor and frequency equation parameters (15).

Thus, in order to determine the strain amplitude in semiconductor wafers, it is necessary to measure the electric field strength $E_{m0} = \frac{U_m}{l_0}$ in the piezoelectric and the resulting Q-factor of the multilayer structure Q_1. Determining the field strength in a piezoelectric at its known thickness is not difficult, and the figure of Q-factor can be measured by the amplitude-frequency response of the current through the piezoelectric plate and use the well-known formula

$$Q_1 = \frac{f_0}{f_2 - f_1},$$

where f_0 is the resonance frequency (maximum current), f_2 and f_1 are the limiting frequencies at which current decreases $\sqrt{2}$ times if compare with the resonance value.

The resonant method of measuring the value of Q-factor is the more accurate the higher the figure of Q-factor. Practically this method can be used if $f_2 - f_1 < 0,05 f_0$, and the appropriate value of Q-factor $Q_1 > 20$. But the control of the intensity of acoustic deformations in order to detect their effect on the quality of ultrasound p-n junctions, we can hope, does not require high accuracy and the resonant method of measuring the figure of Q-factor can be applied at lower figure of Q-factor.

Summary

1. The symmetric and asymmetric multilayer structures of a semiconductor-piezoelectric are analyzed on the basis of a model of a “thin and wide” plate and approximate expressions are obtained for maximum deformation in a silicon wafer as a function of the material properties of a semiconductor and piezoelectric material and their structural features.

2. It is shown that in an asymmetric structure the efficiency of converting the electric excitation voltage of a piezoelectric plate into mechanical deformations of a semiconductor is approximately 30% higher than in a symmetrical structure.

3. Mathematical models of the processes of introduction of dynamic ultrasound oscillations into ion-implanted silicon wafers by static clamping to a piezoelectric plate with subsequent excitation of high frequency ultrasound oscillations in a multilayer structure of a semiconductor-piezoelectric with an electrical voltage applied to piezoelectric plate.

4. The comparison of thermal energy density and thermal expansion of silicon during annealing with the corresponding indicators during acoustic excitation is made, which shows a significant excess of the former over the latter. It follows that a combination of thermal and acoustic treatments may prove to be more effective than each of them individually.

5. A method for determining the intensity of mechanical deformations of semiconductor wafers by recalculating the measurements of the resultant figure of Q factor of the multilayer structure and the electric field strength in the piezoplate is proposed.

The obtained results may be used for control and measuring techniques [12].

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