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Rank differences of signals by weighing-selection processing method for implementation of multifunctional image processing processor

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ABSTRACT

In this paper, we proposed a new iterative process of sorting an array of signals, which differs from the known structures of sorting signals by uniformity, versatility, which allows direct and inverse sorting of an array of analog or digital signals. The basic elements of the proposed sorting structures are simple relational nodes. Such elements can be implemented on a different element basis, including, on devices for selecting a maximum or minimum of two analog or digital signals, which are implemented on CMOS current mirrors and carry out the limited difference function of continuous logic. We offered implementation of homogeneous sorting structure on such elements, consisting of two layers and a multichannel sampling and holding device. Nine signals corresponding to a selection window of a matrix sensor are fed to this structure, we sort them in five iterative steps, and at the output we receive the signals sorted by the rank, which, using the code controlled programmable multiplexer, generates an output signal, corresponding to the selected rank. We evaluated the technical parameters of such a relational preprocessor. The base cells consist of no more than 20 CMOS 1.5μm transistors, the total power consumption of the sorting node on 10 continuously logical base cells (CL BC) is 2mW, the supply voltage is 1.8÷3.3V, the range of an input photocurrent is 0.1÷24μA, the conversion cycle is 10μs. The paper considers results of design and modeling of CL BC based on current mirrors (CM) for creating picture type image processors (IP) with matrix parallel inputs-outputs. Such sorting nodes based on them have a number of advantages: high speed and reliability, simplicity, small power consumption, high integration level. The inclusion of an iterative node for sorting signals into a modified nonlinear IP structure makes it possible to significantly simplify its design and increase the functional capabilities of such processor. The simulation results confirm the proposed approaches to the design of sorting nodes of analog signals of the iterative type, which simplify the complexity of the nodes by an order of magnitude, ensuring their uniformity, regularity and simplicity of scaling. The power consumption of the processors does not exceed 2mW, the response and processing times are 10μs and can be less by an order of magnitude, the supply voltage is 1.8÷3.3V, and the operating currents are optimally in the range of 10÷20μA. The energy efficiency of the proposed preprocessor with the iterative sorting node is $25x10^9$ op / s · W, which corresponds to the best technical solutions. In the work we are shown, that after sorting or comparative analysis of signals by levels of selected window of image, a promising opportunity appears to implement image processors with enhanced functionality using the new method of weighting-selecting rank differences of signals. The essence of the method is that by composing the differences of the signals ordered by rank and the upper level of their range, we can simultaneously form several resulting output signals, choosing the necessary difference signals from their set according to the control commands and weighing them additionally before the summation. We are shown that using this approach and the method of processing the current window signals significantly expands the set of operations and functions for filtering images, simplifying hardware implementation of IP, especially for analog and mixed technologies. We determined set of basic possible executable instruction-functions by processors based on such a proposed method, presenting the simulation results in Mathcad, PSpice OrCad and other environments. We discussed the comparative evaluation of various modifications and options for implementing processor. We analyzed the new approach for the programmable choice of its function or set of functions, including the choice of the required differences between the ranks of signals and their weights. We show the results of design and modeling the proposed new FPGA-implementations of MIP. Simulation results show that processing time in such circuits does not exceed 25 nanoseconds. Circuits are simple, have low supply voltage (2.5 V), low power consumption (50mW), digital accuracy. Calculations show that when using an Altera FPGA chip EP3C16F484 Cyclone III family, it is possible to implement MIP with register memory for image size of 64*64 and window 3*3 in the one chip. For the chip for 2.5V and clock frequency 200MHz the power consumption will be at the level of 200mW, and the calculation time for pixel of filters will be at the level of 25ns.

Keywords: analog relational preprocessor, image nonlinear processing, simulation, continuous logic, current mirror, sorting networks, methods of selection and rank preprocessing, rank filtering.

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1. INTRODUCTION

Intelligent optical detectors based on photodiodes or intelligent optical sensors that can be seamlessly integrated with digital electronics in silicon, which greatly simplifies the design of OE-VLSI circuits and allows you to implement a stacked architecture of a three-dimensional chip, demonstrate a large scope and market potential[1-3]. Since smart detector circuits can be made from almost any semiconductor fabric[1-2], and many demonstration systems have already been created to prove the use of optics or optoelectronics for external and internal microcircuits, our approach prefers an intelligent pixel-like architecture[3-13]. that combines parallel signal detection with parallel processing signals in one circuit, when each pixel has its own analog and analog-to-digital node, which guarantees the fastest processing. Parallel high-speed processing of a 1D or 2-D array using non-traditional MIMO systems, the corresponding matrix logics (multi-valued, continuous, neural-fuzzy and others) and the corresponding mathematical apparatus becomes a strategic direction[4÷23]. By the variety and scope of applications in the most diverse areas of science and technology, not to mention information technology, Boolean two-digit logic covers the entire binary-discrete (virtual) world and therefore the 20th century can rightly be called Boolean. But in the overwhelming majority of cases, various production processes and technologies of the physical macro-world, especially technologies associated with measurement and control processes, are accompanied not by discrete, but by accompanying continual (continuous analog) processes and signals, which leads to contradictions in the use of discrete logics in the continuum[14]. Therefore, for the description and modeling of each continual subject domain and the class of its tasks, its own logical-algebraic apparatus is required. Logic-algebraic (LA) calculi are mathematical (symbolic) domain-oriented logics and special algebras, the formal apparatus of which is based on clear rules that allow you to make an exact description of a certain class of problems and even suggest an algorithm for solving them. For the successful development of continual information technologies and artificial intelligence[15, 16] it is necessary to increase the semantic power of LA-calculus. And for this, both philosophically and mathematically, it is necessary to define their new basic definitions, concepts and, at least on an intuitive level, using them to describe and model the machine-mechanical analogs of thinking processes[17]. The basis of information technologies in the analog field is precisely the continual LA calculus: Lukasiewicz's infinite-valued logic[18], continuous logic with all its variants and generalizations[19, 20], additive-multiplicative logic (AM) algebra[21], predicate selection algebra[22], equivalence algebra[23] and others. They determined the continual biologically inspired stage of development of LA-calculus and a new, more energy-efficient, direction of building models and their hardware implementations of artificial intelligence. Many logics are based on multi-place, multi-input mini-max operations: min (x_1, x_2,…. x_n) and max (x_1, x_2, …. x_n), when defining variables on a unit interval[19, 20] : $x_i \in [0,1]$. Note that many models and image processing algorithms, artificial neural-fuzzy systems, their basic procedures of composition-decomposition and fuzzy inference are also based on such multi-input mini-max operations. Therefore, there is an urgent need to improve the hardware implementations of nodes that perform these and similar operations, especially for those applications where the number of operations and input variables are significant. Arrays of matrix elements of continuous and threshold, rank, and order logic are also required for promising implementations of future computing architectures based on 3D chips, including optical training neural networks (NN) with a two-dimensional structure[4], equivalence models (CLEM) NN[5÷7], especially to create convolutional and new self-learning equivalence-convolutional structures[24-27]. The use of architectures with time-pulse-coded analog variables (TPCA), which were considered in works[6, 7, 8, 10, 12] and based on a generalized unified methodological basis for creating a whole family of universal (multifunctional) elements of various logics, although they provide many advantages regarding the expansion of the set of functions and their programmable samples do not satisfy the time requirements while maintaining a satisfactory dynamic range in terms of accuracy. Such a time-pulse-encoded representation of matrix continuous logic variables by two-level signals, although it allows you to expand the functionality and simplify the tuning circuit for the required function, does not satisfy the increased requirements for speed and accuracy of calculations. In works[7, 8, 11, 12] the fundamentals of designing universal (multifunctional) logic elements (ULE) of a matrix logical structure with fast programmable tuning were considered. Consider a brief overview, the motivation for designing a multifunctional image processing processor. A special place among the methods of effective high-speed image processing working with arrays is occupied by the class of structured nonlinear methods and algorithms that performed the conversion of the form:

$$\mathbf{B}=\{b_{ke}\}=\mathbf{F}(\mathbf{A})=\{\mathbf{\Phi}_{kl}(\mathbf{A}_{kl})\},$$

where $\mathbf{\Phi}_{kl}(\mathbf{A}_{kl})$ — nonlinear function which is determined by subset of rank and (or) index statistician of selection. It is formed by signal samples from some neighboring of this element in the sequence of the well-organized samples of signal, and it is named as variational series[28]. By virtue of the last this subclass was adopted by rank algorithms. The algorithms of extreme filtration, using values of minimum and maximum on samples of neighborhood space, are the special cases of the rank algorithms. Any r-th index statisticians $v_s(\mathbf{r})$ of display (k, l) the set neighboring of which form

other (N_s-1) the elements of selection it is possible to bind to the local histograms of distributing of values of neighboring elements and with the proper functions of the well-organized choice $F_n^m \vec{x}$ ($\vec{x}$) element, where $\vec{x}$ =(x_1, x_2, …. x_n). Such functions at any values of changing variables choose that size which at the location all right not decreasing are occupied by m-th place. These functions can be represented by a logical formula[19]:

$F_n^m(x)=\max\limits_{1\le i,<\ldots<i_{n-m+1}\le n}[\min(Xi_{1,\ldots}Xi_{n-m+1})]$, or $f^{(r)}(x_1,\ldots x_n)=x^{(r)}$, $r=\overline{1,n}$,

where r-rank of the base operations of continuous logic (CL)[20]. Index operations are used with operations of denial, addition. Thus for r = n this operation passes to n-local disjunction, for r=1 to n-local conjunction. As examples of functions of ordinal logic can be the median and inversion of the median, as well as a number of others[20]. The algebra formed in a number of C = [0, 1] with base operations f(r) and (-) is named ordering Boolean algebra. The row of specific laws is inherent to it: tautology, commutative, distributive[20]. Rank algorithms are locally-adaptive on the same essence: simplicity of local adaptation, invariance to spatial links and to signals dimension, almost algorithms complication independence from the sizes of neighboring. Also, at calculation of concrete rank statistician and derivative the further simplifications related to informative surplus of images are possible. In paper[29] approaches to creation of classifiers of the distributed ensembles of continuous signals were shown. The distributions of their amplitudes were used to evaluate the characteristics of classified objects and classifiers that control and compare the correlations of the so-called lattice functions based on a hierarchical description of the shape. Such descriptions in terms of more than or equal to, less than or equal to, or in terms of more, less, and the same, also require the use of similar operations of order logic and the like. The proposed models of neuron classifiers and identification algorithms based on a hierarchical description of the forms of lattice functions allow one to theoretically quite subtly isolate and compare these forms. Estimates of the number of potentially distinguished forms show that such multilayer neural recognizer classifiers with n inputs and (n-2) layers (according to classification levels) can have high accuracy of multilayer classification. Thus, analysis of foregoing allows drawing conclusion about the necessity of development of hardware sorting devices with the sufficient number of inputs (executing «ordering» of input values and supervisory after the well-organized locations (variables). Taking to account that at the proper transpositions, the common number of combinations of all links is very great, clearly that the use of new technologies is the decision of problem. Known base cells, that forms such converter-orders[29]. They are executed as association of two logical charts: charts of selecting of a less value min(x1, x2) and charts of function max(x1, x2). Also well-known wave structures that are completely homogeneous with regular connections are based on such basic cells that order the ranking of the analog or digital variables[29]. The continuously logical (CL) – transformations are shown in paper[30, 31], in which the transformation CL functions (CLF) are defined and it is shown that the operation of min, max of continuous logic are the basic operations of the functions. Use of operators of hybrid logic for formation of CLF it is possible: $D_1[P(x1,x2)]=\max(x_1,x_2)$, $D_2[P(x1,x2)]=\min(x_1,x_2)$, where P and D are respectively the threshold and the de-threshold operators, which are realized by various means. Besides, in works[30, 31] it has been shown that some operations of continuous logic, such as equivalence and nonequivalence, and their generalized family, allow to receive a number of advantages in so identified «equivalence to a paradigm» neural-network models. These scalar operations of equivalence eq (x, y) and nonequivalence neq (x, y) for x, y ∈ [0,1] are defined in works[6, 7], namely: $eq(x,y)= x\Lambda y+\bar{x}\Lambda\bar{y}=\min(x,y)+\min\big((1-x),(1-y)\big)=1-|x-y|$, $neq(x,y)=|x-y|=1-eq(x,y)=$ $=\max(x,y)-\min(x,y)=\max(\bar{x},\bar{y})-\min(\bar{x},\bar{y})=(x\div y)+(y\div x)$, where (÷) - is the operation of a limited difference. If we consider that at $y=1\div x=\bar{x}$, these functions are transformed to: eq (x, $\bar{x}$) = 2(x ∧ $\bar{x}$) = 2min(x, $\bar{x}$), neq(x, $\bar{x}$) = max(x, $\bar{x}$) - min(x, $\bar{x}$) = 1- 2min(x, $\bar{x}$), as has been shown in work[30], these functions can be successfully used in CL ADC. The use of CL-transformations and CLF made it possible to create promising energy-efficient analog-to-digital converters for intelligent detectors on their basis[30, 31, 32]. In many neural-network models for recognition of gray images it is desirable to have picture binary bit-planes, which encode the image matrix in Gray codes. And for this, the CL-ADC with the Gray code is suitable. In realization of equivalence models[3, 5, 23] and scalar-relation processors[10] in every channel it is necessary to realize component-wise equivalence operations of type: $a_i\tilde{\vee}b_i$ $a_i\not\tilde{\vee}b_i$ and other types for which the maximum and minimum values or their differences are required. They also require of variables ranging $a_i,\bar{a}_i,b_i,\bar{b}_i$, represented by optical signals and will realize min and max operations on from 2 to 4 variables. But the implementation of such continuously logical base cells (CL_BCs), which perform the operations min (x1, x2) and max (x1, x2), is rather complicated for digital variables[19]. And the CL BC based on current mirrors (CMs), proposed in work[30], although simple, only 13 CMOS transistors, their number to build a traditional know wave network structure of such cells, especially at large values ($n\approx 9\div 25$), is very large. At the same time, an increase in the depth of the

structure, the number of layers of CL BCs, all the same increases both the complexity and the sorting time. But at the same time with an increase in the number of analog cells accuracy decreases, so more accurate digital implementations need to be sought.

To create fully parallel algorithms and tools for image processors[31, 32, 33] morphological image processing[34-37], especially for implementing such basic operations as dilation, erosion, opening, closing[37], etc., the above mentioned min-max operations on sets of signals are also necessary, which represent structural windows or selected fragments processed images. Many of the above-mentioned morphological operations need to be repeated many times and for all the current fragments of the image being processed, therefore, there is an urgent need to reduce the execution time and the underlying min-max operations and ranking operations. Sorting algorithms have been widely researched due to the need for sorting in many applications [38-41]. Sorting algorithms have been specialized for particular sorting situations, such as, high-speed sorting[42], sorting using a single CPU and multiple CPUs, parallel image and big data processing[43]. To create more advanced intelligent sensors and image processing processors[32,33] with enhanced functionality and combining analog or analog-digital preprocessing of signals in a dedicated and accessible structural area (window) also requires sampling, storage, sorting and selection of signals. In papers[44, 45] approaches to creation of programmable relational optoelectronic time-pulse coded processors as base elements for sorting neural networks were shown. But in such a relational optoelectronic processor, working with analog signals both amplitude-coded and time-pulse-coded, the sorting structure for ordering signals is complex, since the number of base cells in the layer and the required number of layers increase proportionally with the number of input variables. Therefore, the goal of our work is to search for compromise new options for implementing both signal sorting nodes, including analog and digital, providing increased accuracy and speed, and based on them relational non-linear image processing processors with advanced functionality. And since such processors can be used as multifunctional nodes of ordinal logic, extremum selectors, nodes of ordering and sorting data, rank filters, recognizers of fragment classifiers, etc., the question of their implementation is acute. In addition, taking into account the recent emergence of a new element base, our task is to prove the possibility of creating on the FPGA, practically in one chip, an image preprocessor (IP) with enhanced technical characteristics and a wide range of commands through the use of a new method of processing pre-ranked signals and (or) their differences. Therefore, the goal of our work is the design and modeling of technical options for the implementation of the main nodes, including the sorting nodes, which significantly expand the functionality and range of tasks solved by multifunctional relational image preprocessors.

2. STRUCTURE DESIGN OF NONLINEAR PROCESSING RELATIONAL PREPROCESSOR BASED ON SORTING NODE

2.1 Structure of the basic relational preprocessor (BRP) of nonlinear image processing

The structure of the basic relational preprocessor (BRP) of nonlinear image processing and its modified conveyor homogeneous with regular connections wave structure (MCHWS), which performs sorting and ordering of analog or digital signals and is one of the main processor nodes, are shown in Fig. 1 and were considered in more detail and described in works[44-46]. In the future, for simplicity, we can call this main unit the sorting unit (SU) of analog or digital signals, the specifics and implementation features of which depend on the type and form of signal representation. The work considered analog processors based on the SU, consisting of a conveyor of layers of selector-rank disjunctive-conjunctive elements (SRDCE). Modified wave structure on the basis of selector-rank disjunctive - conjunctive elements (SRDCE) using the continuous logic base analog cell with many ordered outputs. Comparative analysis of structures of ranging of analog signals (SRAS) by traditional approaches done by us shows the wave structures require less of equipment, along with other advantages (regularity, homogeneity, base cells only of 2 forms and 2 CLFs). This winning is especially and is increased at growth of number of variables n. Therefore our approach oriented to wave structure is special important at considerable n and provides integration at the requirement of multi-channeling of such devices. From other side at time-pulse coding of the element min and max CL variables (TPCV) is taken to implementation of the operations "AND" and "OR" of two-valued logic. This allows you to use only the simplest two-input AND elements and two-input OR elements for SRDCE to implement time-pulse coding of CL-variables[44]. In Fig. 2 shows an SRDCE circuit that is known and modified to better match currents in and out. The cell circuits of only 13 CMOS transistors, and adding 4 or 6 transistors to them, which compare the currents, it is easy to get a digital potential output of the comparator. The SRDCE as base cell executing organization of two analog optical signals that in fact is two photocurrents was designed and simulated[45, 47]. The results[45] of operation of such cell are following: range of the input photocurrents 0.1÷40μA, supply voltage is 1.8÷3.3V, duration of fronts 20÷100ns, total delays no more than 200ns. Such cells are enough simple (only 13 transistors). At complication they can be more high exactness. As can be seen from Fig. 1, the well-known wave structure[44, 45] has (n-1) layers consisting of completely identical base cells, the number of which is determined by

rounding to integer {n/2}, where n is the number of input variables. If this number is an even number, for example, n = 6, then in each of the five layers there will be 3 basic cells, and there will be 15 of them in total (Fig. 1). For n = 4, there will be 6 base cells in all three layers. Note that for more homogeneity and regularity of bonds in the structure, it is advisable to choose n even. Therefore, for image processing, even with a minimum window size of 3x3, it is necessary to make a structure of 45 basic cells, since: (10/2)x(10-1) = 45. It can be shown that when introducing the tenth input as a control (with the value of the lower or upper boundary of the range of processed signals), the number of necessary permutations for ordering nine signals from the pixels of the current window decreases to 8, which means that the number of layers can be as little as 8. But all the same time, the number of all cells for the 3x3 window will decrease only to 40. Already with a window of 7x7, you will need ((49+ 1) / 2) x (49-1) = 25x48 = 1200 cells, which greatly complicates the structure. In addition, due to the increase in the number of layers, the delay time of signals and errors due to their accumulation also increase. A supporting example is the following.

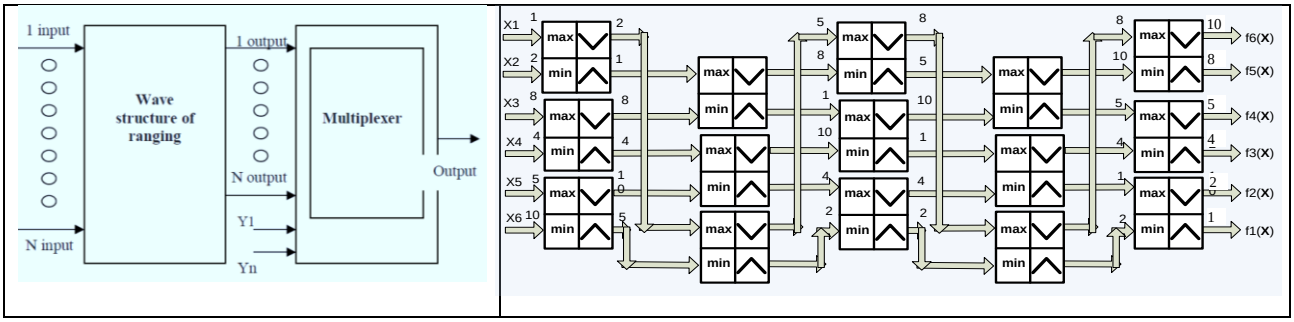

Fig. 1. Structure (left) of BRP with N inputs and output; SU based on MCHWS (right) for n =6 (SU have n-1=5 layers consisting of completely identical base cells SRDCE

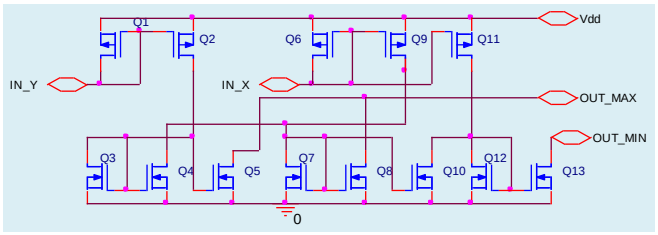

Fig. 2 The modified continuous logic base analog cell for wave sorting structure: Selector-rank disjunctive - conjunctive element based on current mirrors with two inputs and two outputs

The 4-input sorting structure of analog signals using of 6 the modified CL BCs based on two-input and two-output SRDCEs is represented in work[44]. It executes sorting of these 4 input signals represented by photocurrents or currents. The circuit is in fact the device of order logic, calculating simultaneously all operations of the proper ranks r = 1÷4. The simulation results[44] of such structure shown, that the structure functions correctly, although error in the levels of signals before and after do not exceed 5 ÷ 6% for currents Dmax =20÷40μA and 1÷3% for currents Dmax = 5÷10μA. The multiplexer (Fig. 1) allows the control code (y1, y2, ..., yn) to choose the rank n and, accordingly, the type of required operation or function. The switch (Fig. 1) allows the control code (y1, y2, ..., yn) to select rank n and, accordingly, the type of operation required. The results of the design and simulation of the programmable relational optoelectronic time-pulse coded processor (PROTPCP)[44], which, unlike the processor in Fig. 1, additionally has a block of pulse-width photo-converters-modulators[47] on currents mirrors showed, that for n = 8 parameters of such PROTPCP the following: processing period - 1÷2μs, $t_{delay\Sigma} \approx 12 \div 14$ns, 56 two-input elements of "AND" or "OR", power of the input optic signals - 0.2-200μW. In Fig. 3 the graphical representation of the processor operations is shown. Fig. 4 shows time diagram of PROTPCP for n=8.

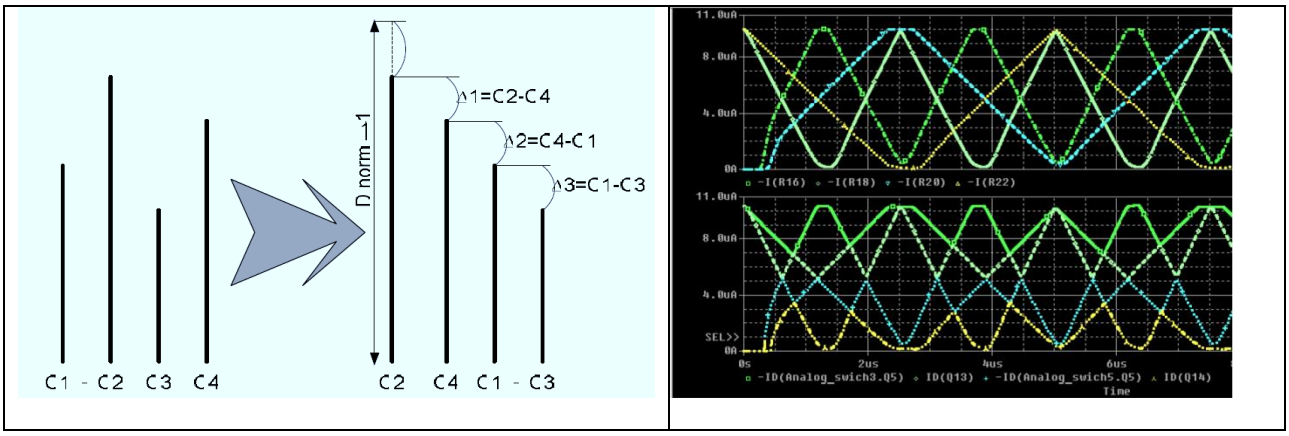

Fig. 3. Graphical representation of the processor operations (left); Simulation results of the 4-input sorting structure of analog signals using of 6 the modified base analog cell based on two-input and two-output selector-rank disjunctive - conjunctive elements for small currents (right)

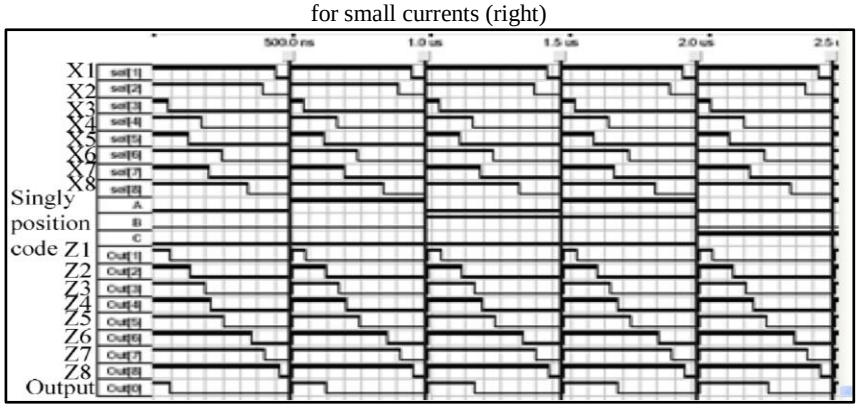

Fig. 4. Time diagram of PROTPCP for n=8 (shows different functions in periods)

Since such processors (Figs. 1, 3) have output signals that are ranked by value and not by difference of values, by some modification[45] they can be used to organize an additional calculation of the difference of signals having neighboring ranks. And the difference in signal values is also necessary for such a function as nonequivalence. Based on the operations of bounded difference and nonequivalence, a whole set of other continuous logic complex operations and functions are constructed. For example, early we can select one of n signals by rank using multiplexer. And now we can also form signals difference between max signal and next by order. So we can find signal that is proportional to difference of any two signals from ordered set. Such approach allows to formed output complement analog signals (Fig. 3). If one of reference level is 1, than difference between the reference and any of signals is the continuous logic complement of the analog signal. A block diagram of such a modified processor for four outputs, a circuit of an internal analog switch and a sub-block for calculating difference and additional analog signals are considered in work[45], where it is shown that such processors can work with both analog and time-pulse-encoded signals.

2.2 Structure of the modified relational preprocessor (MRP) with iterative sorting node[45]

The modified iterative sorting structure based on a multichannel sampling and storage device and two linear arrays, consisting of basic continuous-logic analog cells (disjunctive-conjunctive elements of the selector rank (SRDCE) with ordered outputs) is shown in Fig. 5. Details of the structure and their base cells will be discussed in the report[45]. The simulation results of proposed MRP with PSpice Orcad are shown in Fig. 6, 7 for different modes of operation of the iterative sorting node. They show that for used 1.5μm CMOS transistors (Ts), the total sorting time of 10 signals (9 input information variables and one auxiliary) with permissible errors does not exceed 6÷18μs (for evaluation, we take 10μs). This time is made up of the five required clocks, but the rewriting beat in the SHD and the read beat can be different. We doubled the last one and therefore the total time was proportional to 6 cycles. The levels of input signals in the figures are indicated by different colors, which allow you to see the dynamic of transitions and the change of signal levels during exchanges, permutations. At the inputs we gave signals, ordered by their levels in the reverse order. This made it possible to more clearly demonstrate the process of ranking in which the signal with the highest level appeared at the top

output of the circuit. Let us estimate the complexity of such a sorting node. Each SHD consists of 16 Ts, there are only 10. And the two lines (layers) of basic cells with min-max operations (comparisons and exchanges in essence!) consist of 10 cells, each of which is performed on 13 Ts. Therefore, the total number of transistors will be equal to: 16x10+13x10= =290. Taking into account the presence of some other auxiliary circuits: clock signal generators, a multiplexer and matching buffers; we can assume that only up to 400 transistors will be needed. Even for the fastest and most advanced algorithms and sorting schemes, the total number of comparison and exchange operations is proportional to (nlogn)x1.5 and for n=10 is about 50. Thus, taking into account that for the simulated circuit the power consumption was 2mWs and Tproc = 10^{-5}s, we obtain for the simultaneous formation of ten output functions the energy efficiency estimate at the level: 500op/(10^{-5}s · 2x10^{-3} W)=25x10^{9} op / s · W. And this means that at least several hundred of them could be placed on the chip. But here the problem of interconnections will appear and the exit from it to ensure parallel inputs will be just an array of photo-detectors. Structure of multichannel 8 bit ADC (1D array 8 bit CL_ADC) with analog signals preprocessing was described in paper[32]. It uses the same SHD, similar cells and iterative approaches, and this allows for additional in such processors to implement anloe-digital transformation, both before and after sorting the signals.

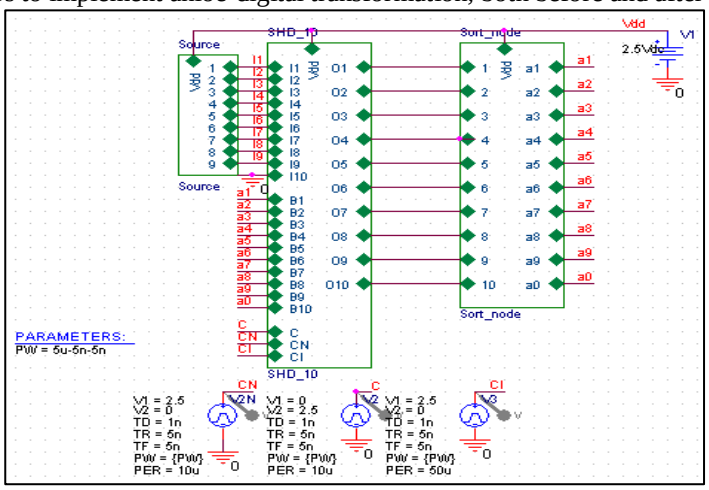

Fig. 5. A modified iterative sorting structure based on a multichannel sampling and storage device and two linear arrays consisting of basic continuous-logic analog cells (disjunctive-conjunctive elements of the selector rank (SRDCE) with ordered outputs).

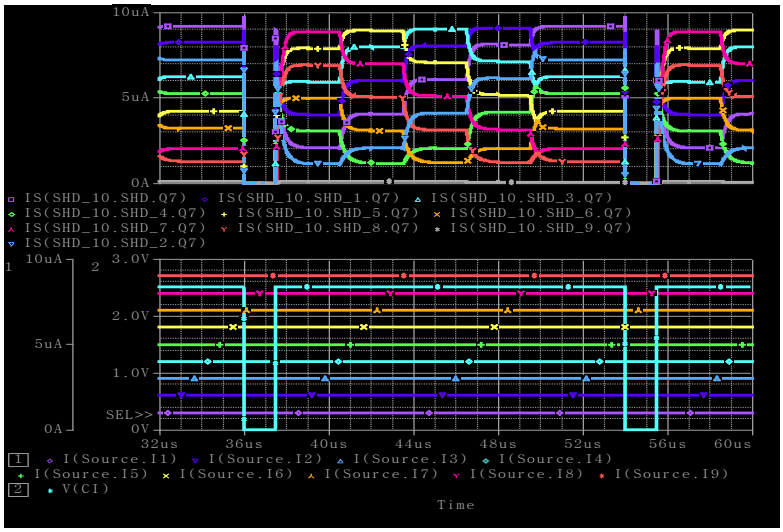

Fig. 6. Simulation results of iterative sorting node for Vdd=2.5V, Dmax=10μA, T=18μs

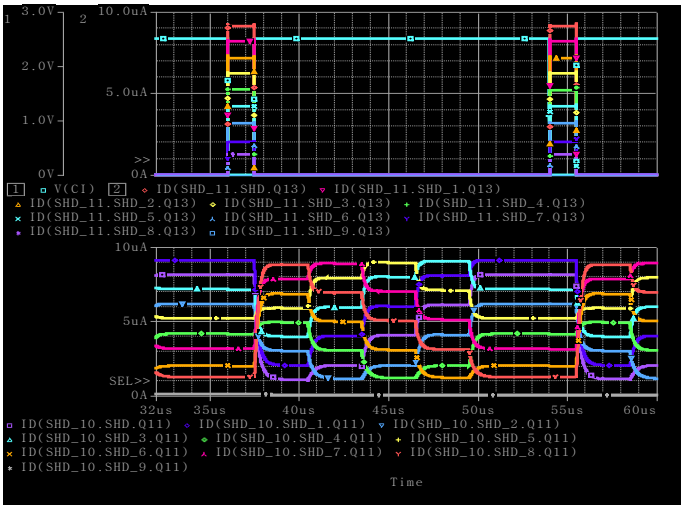

Fig. 7. Simulation results of iterative sorting node for Vdd=2.5V, Dmax=10μA, T=18μs in the case of one ramp / falling signal and nine constants

3. DESIGN AND SIMULATION OF MULTIFUNCTIONAL IMAGE PROCESSING PROCESSOR (MIP) BASED ON FPGA AND USED METHOD OF PROCESSING WEIGHTING-SELECTING SIGNALS OF RANK DIFFERENCES

3.1 Rank differences signals weighing-selection processing method

The essence of the proposed method is as follows. The signals of the selected current WAG window 3x3 in size, corresponding to the tx, ty-pixel $Amo_{tx,\ ty}$ of some image, are fed to the input of the sorting node and ordered signals V_sor0-V-sor8 are formed at its outputs, which are denoted as Ds (r) where r is the rank. These signals corresponding to the ranks, using the control vector Y are selected (weighed) by the switching node in accordance with the formula:

$$\mathbf{Fs\_Am(Y)} := \sum_{\mathbf{r}=0}^{9} \mathbf{Y_r \cdot Ds(r)}$$

Similarly, from the calculated (Dr0 = D - V_sor0, Dr1 = V_sor0– V_sor1, Dr2 = V_sor1– V_sor2, ... Dr8 = V_sor7– V_sor8, Dr9 = V_sor8) rank differences, denoted by Dr (r), are selected using the similar control vector Y (weighed), if necessary, the second switching node in accordance with the formula:

$$\mathbf{F\_Am(Y)} := \sum_{\mathbf{r}=0}^{9} \mathbf{Y_r \cdot Dr(r)}$$

Examples of control vectors and a specific example of a window with signals to be processed, with the results obtained for it for different vectors with explanatory calculations, are shown in Fig. 8, 9. It can be seen from them that a significant number of functions, operations from window signals, including any selected rank, the difference of the selected ranks, addition to the signal, weighted sums of the selected ranks, etc. can be generated at the processor output. Thus, taking into account especially simple implementations of the operations of summation-subtraction, both for digital and analog signals, the proposed method significantly simplifies the implementation and extends the functionality, set of operations.

3.2 Simulation of a multifunction processor

Structure of MIP based on FPGA with 10 inputs and 1 output; SU based on MCHWS consisting of layers of digital comparison switching circuits is shown in Fig.10 and simulation results are shown in Fig. 11. Here, at first, a variant with one output and supply of all input signals in parallel is shown. For the convenience of data input, we have developed and modeled a processor circuit with register memory for fast sequential image input and automatic sequential search of processed windows. It is shown in Fig. 12. There is only one way out (ranks). The simulation results are shown in Fig. 13-20. As can be seen from Fig. 13, 17 the resources of the Altera FPGA chip EP3C16F484 Cyclone III family are not fully used in the first case, and in the second for the processor with register memory and two outputs almost completely (there is a small margin). The processing cycle in the pipelined structure of MIP and SU did not exceed 25 nanoseconds, which makes it possible to achieve an input / output rate of pixels of the processed and processed images at the level of 40 MHz. During the processing cycle, MIP essentially performs (9 * ln9-estimates for the best algorithms!) Sorting operations and generates all the ranks and their differences, which gives, taking into account the wide variety of output functions, performance estimates of at least 10^9 operations per second.

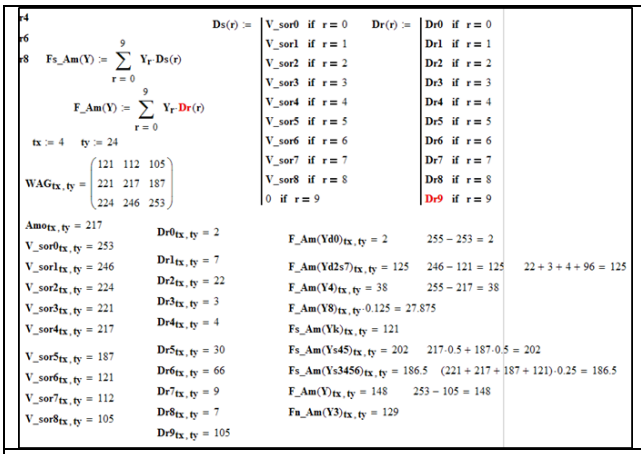

Fig. 8. Simulation of MIP (An example of processing a window in Mathcad)

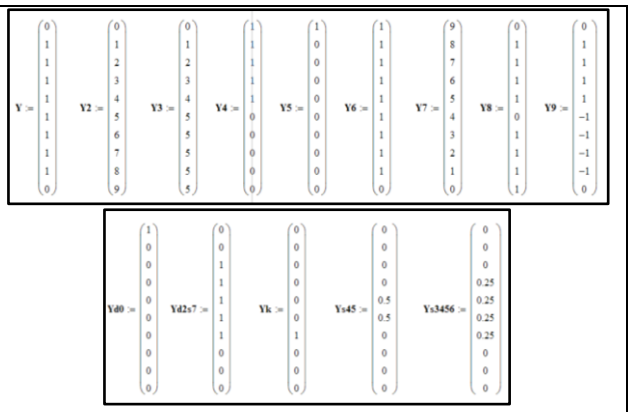

Fig. 9. Simulation of MIP based on FPGA (CPU control vectors)

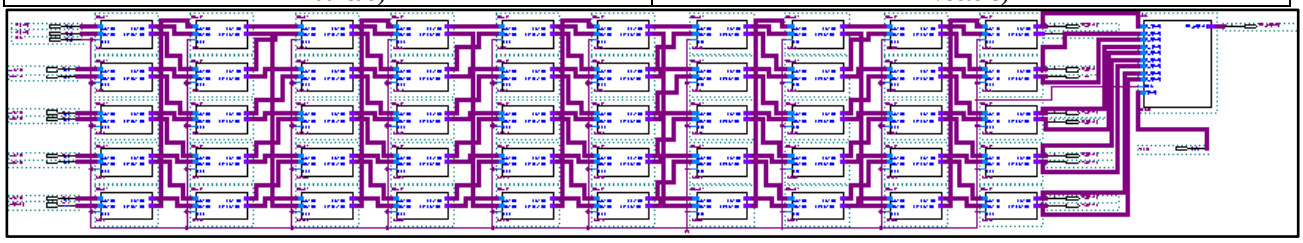

Fig. 10. Structure of MIP based on FPGA with 10 inputs and 1 output; SU based on MCHWS consisting of layers of digital comparison switching circuits

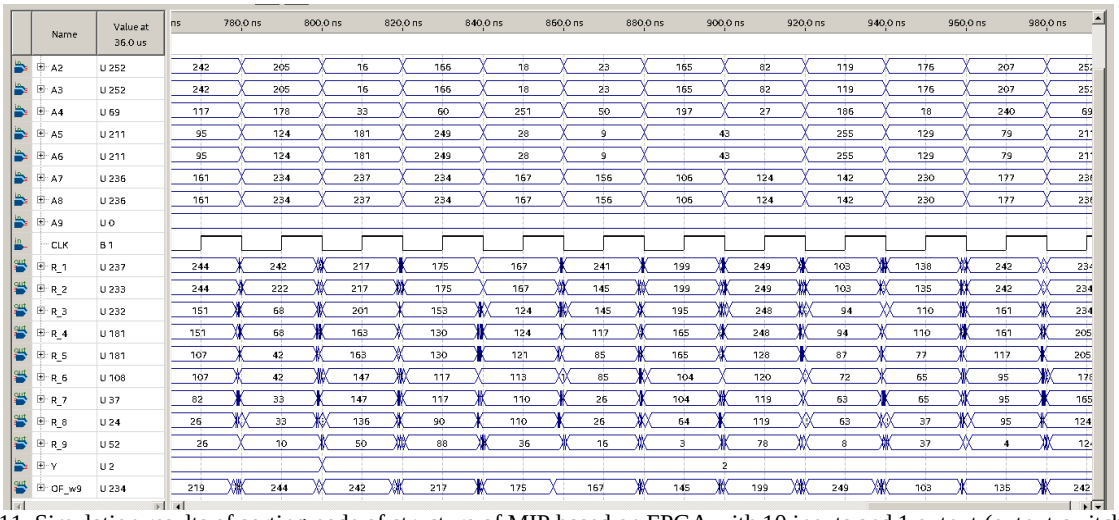

Fig. 11. Simulation results of sorting node of structure of MIP based on FPGA with 10 inputs and 1 output (output switching)

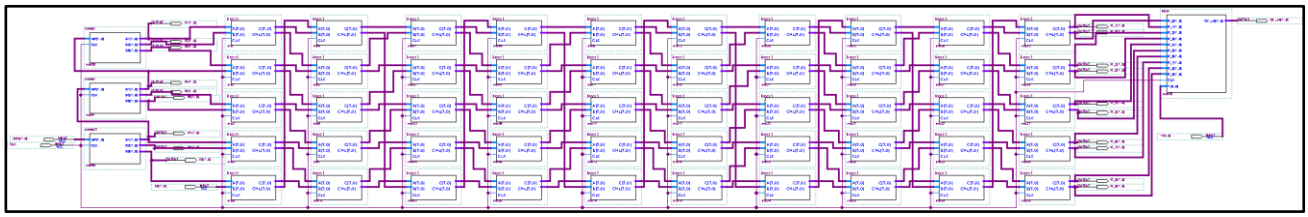

Fig. 12. Structure of MIP based on FPGA with 10 inputs and 1 output with register memory

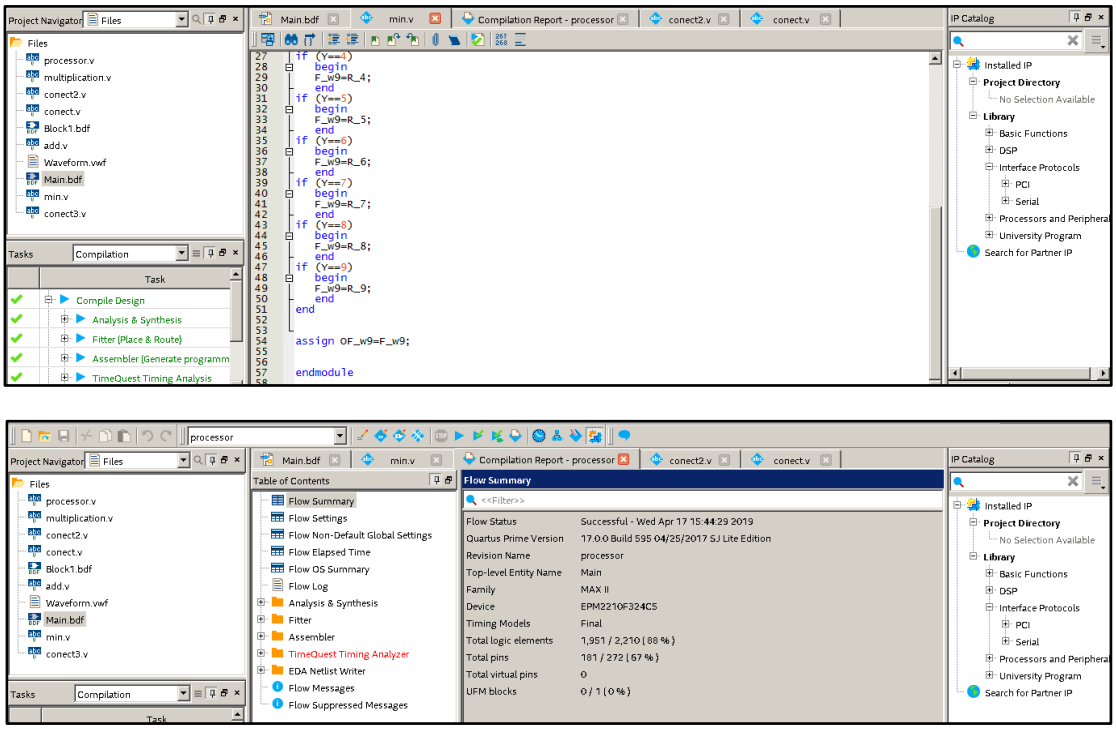

Fig. 13. Simulation of Structure of MIP based on FPGA (window fragments)

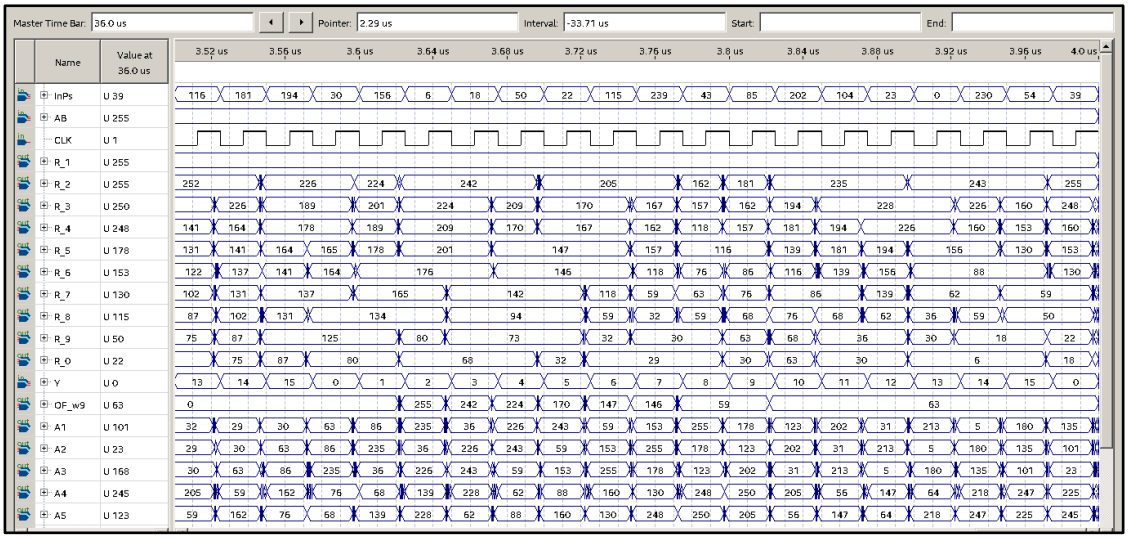

Fig. 14. Simulation results of sorting node of structure of MIP based on FPGA with 10 inputs and 1 output (issuing ranks, one switch)

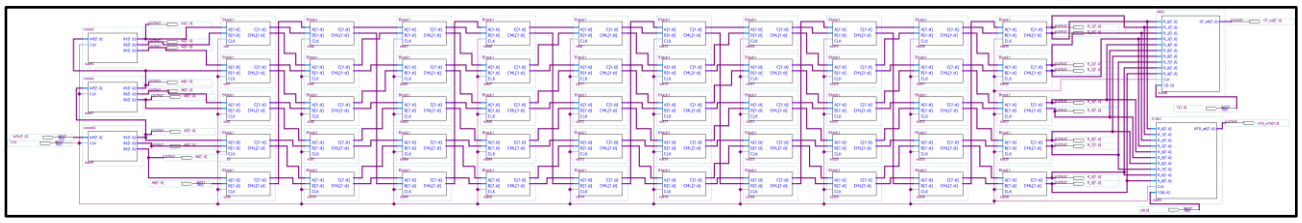

Fig. 15. Structure of MIP based on FPGA with 10 inputs, 2 output and with register memory

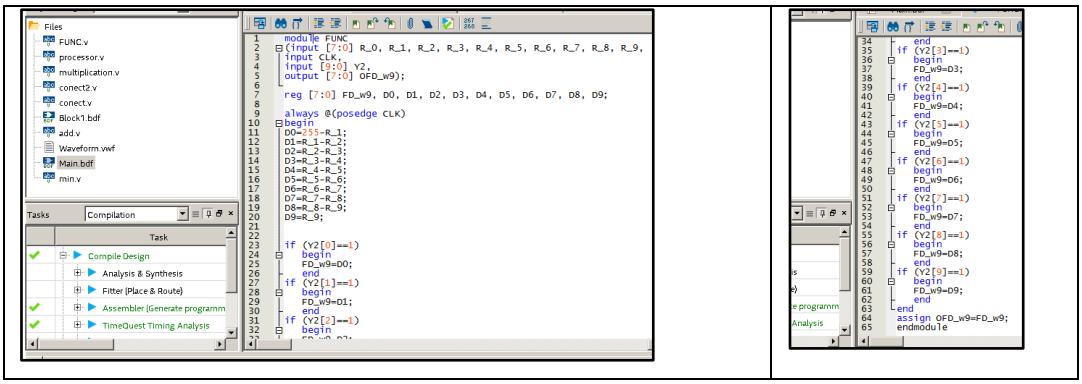

Fig. 16. Simulation of structure of MIP based on FPGA with 10 inputs and 2 output (window fragments, unit design listings)

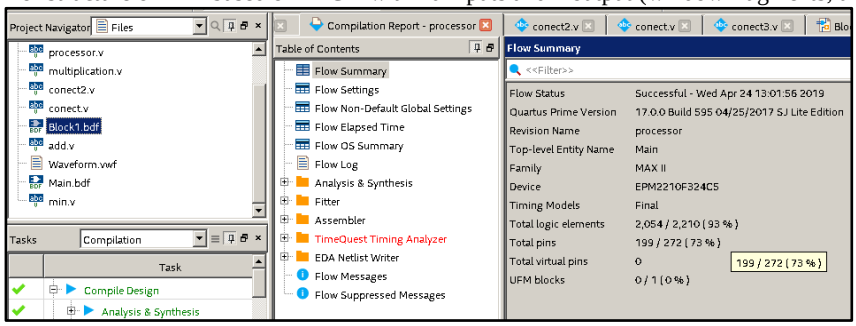

Fig. 17. Simulation of MIP based on FPGA with 10 inputs and 2 output (window fragments)

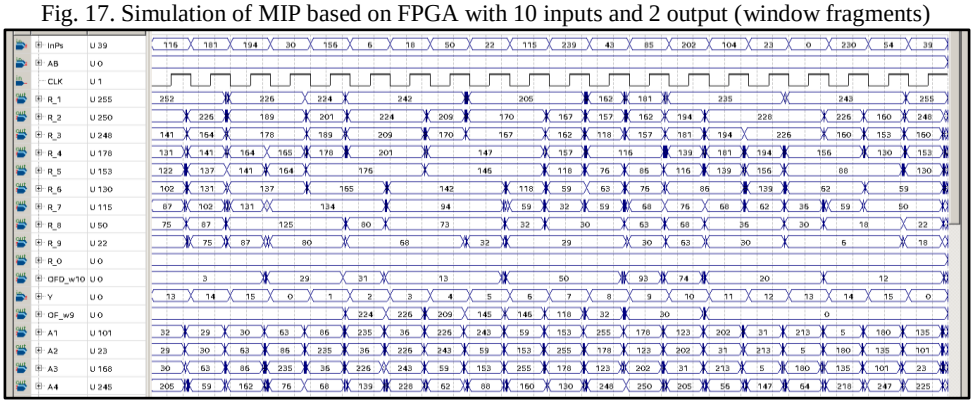

Fig. 18. Simulation of MIP based on FPGA with 10 inputs and 1 output (issuing ranks, two commutators) In the case of the formation of additions to the largest at the second output.

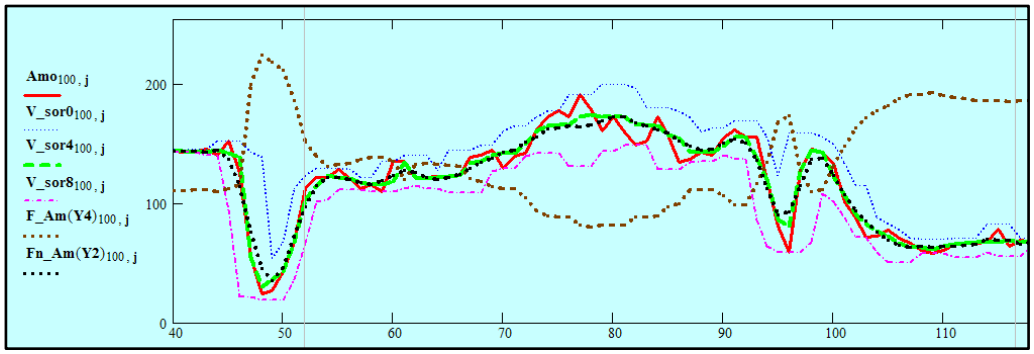

Fig. 19. A good example of processing using an MIP image line (Matcad Window): Original line (red) and received rank and other output functions.

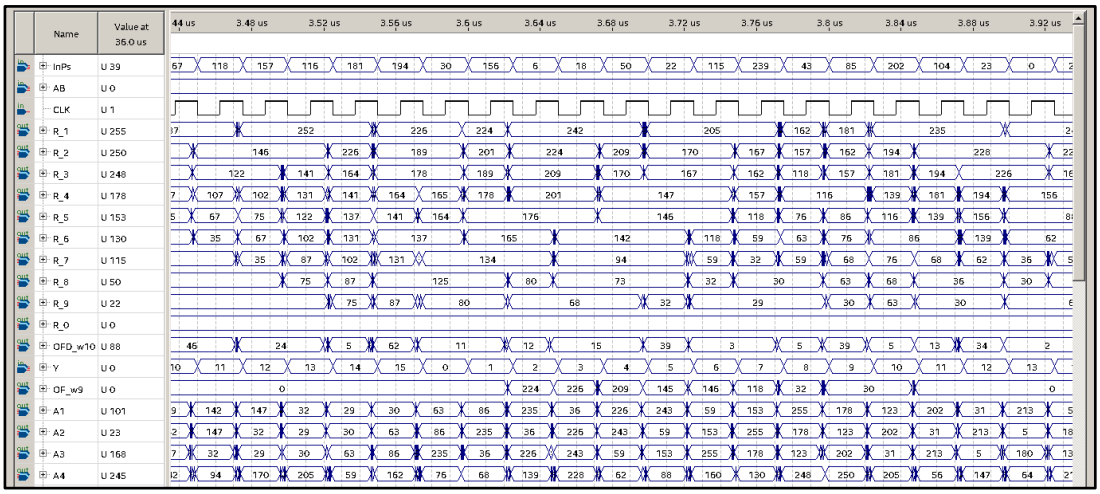

Fig. 20. Simulation results of sorting node of structure of MIP based on FPGA with 10 inputs and 1 output (issuing ranks, two switches) In case of formation of a difference of ranks r2-r3

CONCLUSIONS

We proposed a new iterative process of sorting an array of signals, which differs from the known structures of sorting signals by uniformity, versatility, which allows direct and inverse sorting of an array of analog or digital signals. The basic elements of the proposed sorting unit (SU) are simple relational nodes. Such elements can be implemented on a different element basis, including, on devices for selecting a maximum or minimum of two analog or digital signals. We offered implementation of homogeneous SU on CL BCs, consisting of two layers and a multichannel SHDs and FPGA. Nine signals corresponding to a selection window of a matrix sensor are fed to this structure, we sort them in five iterative steps, and at the output we receive the signals sorted by the rank, which, using the code controlled programmable multiplexer, generates an output signal, corresponding to the selected rank. We evaluated the technical parameters of such a relational preprocessor. The CL BC on current mirrors (CM) consist of no more than 20 CMOS transistors, the total power consumption of the sorting node on 10 cells is 2mW, the supply voltage is 1.8÷3.3V, the range of an input current is 0.1÷24μA, the conversion cycle is 10μs. Such SU for creating picture type image processors (IP) with matrix parallel inputs-outputs have a number of advantages: high speed and reliability, simplicity, small power consumption, high integration level. The inclusion of an iterative node for sorting signals into a modified nonlinear IP structure makes it possible to significantly simplify its design and increase the functional capabilities of such IP. The simulation results confirm the proposed approaches to the design of SUs of analog signals of the iterative type, which simplify the complexity of the nodes by an order of magnitude, ensuring their uniformity, regularity and simplicity of scaling. The power consumption of the IPs does not exceed 2mW, the response and processing times are 10μs and can be less by an order of magnitude, the supply voltage is 1.8÷3.3V, and the operating currents are optimally in the range of 10÷20μA. The energy efficiency of the proposed preprocessor with the iterative SU is $25x10^9$ op / s · W, which corresponds to the best technical solutions. In the work we are shown, that after sorting or comparative analysis of signals by levels of selected window of image, a promising opportunity appears to implement MIPs with enhanced functionality using the new method of weighting-selecting rank differences of signals. The essence of the method is that by composing the differences of the signals ordered by rank and the upper level of their range, we can simultaneously form several resulting output signals, choosing the necessary difference signals from their set according to the control commands and weighing them additionally before the summation. We are shown that using this approach of processing the current window signals significantly expands the set of operations and functions for filtering images, simplifying hardware implementation of MIP, especially for analog and mixed technologies. We determined set of basic possible executable instruction-functions by processors based on such a proposed method, presenting the simulation results. We show the results of design and modeling the proposed new FPGA-implementations of MIP. Simulation results show that processing time in such circuits does not exceed 25 nanoseconds. Circuits are simple, have low supply voltage (2.5 V), low power consumption (50mW), digital accuracy. Calculations show that when using an Altera FPGA chip EP3C16F484 Cyclone III family, it is possible to implement MIP with register memory for image size of 64*64 and window 3*3 in the one chip. For the chip for 2.5V and clock frequency 200MHz the power consumption will be at the level of 200mW, and the calculation time for pixel of filters will be at the level of 25ns.

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