CEUR-WS.org Management Team

The management team is responsible for the service and its development.
The team also checks the compliance of submissions with our publication criteria.

Ilaria Tiddi
Editor-in-Chief
Vrije Universiteit Amsterdam, The Netherlands

responsible for the CEUR-WS.org service, its rules, and its strategy; also manages the main publication service of CEUR-WS.org and interacts with volume editors

Matteo Baldoni
Associate Editor
University of Turin, Italy

responsible for the AI*IA subseries at CEUR-WS.org

Oliver Kutz
Associate Editor
Free University of Bozen/Bolzano, Italy

responsible for the IAOA subseries at CEUR-WS.org

Dmitry S. Kulyabov
Associate Editor
Peoples' Friendship University of Russia, Moscow, Russia

works on the main publication service and interacts with volume editors; maintains the CEURART style for papers published at CEUR-WS

Maria Gäde
Associate Editor
Humboldt-Universität zu Berlin, Germany

works on the main publication service and interacts with volume editors

Michael Cochez
Associate and Technical Editor
Vrije Universiteit Amsterdam, The Netherlands

works on the main publication service and interacts with volume editors; manages the CEUR-WS ticket system

Roberto Micalizio
Associate Editor
University of Turin, Italy

works on the main publication service and interacts with volume editors

Angelo Salatino
Associate Editor
The Open University, United Kingdom

works on the main publication service and interacts with volume editors

Anna Kalenkova
Associate Editor
The University of Adelaide, Australia

works on the main publication service and interacts with volume editors

Maria Magdalena Hedblom
Associate Editor
Jönköping School of Engineering, Sweden

works on the main publication service and interacts with volume editors

Davide Dell'Anna
Associate Editor
Utrecht University, The Netherlands

works on the main publication service and interacts with volume editors

Hector Florez
Associate Editor
Universidad Distrital Francisco Jose de Caldas, Colombia

works on the main publication service and interacts with volume editors

Christoph Lange
Technical Editor
Fraunhofer Institute for Applied Information Technology FIT / RWTH Aachen University, Germany

workflow automation and interoperability with external services

Wolfgang Fahl
Technical Editor
RWTH Aachen University, Germany

workflow automation and interoperability with external services

CEUR-WS.org Advisory Team

The advisory team assists the management team in strategic questions and supervises the quality of the service. It also appoints the editor-in-chief of the service.

Manfred Jeusfeld
Chair of Advisory Team
University of Skövde, Sweden

founder of CEUR-WS.org; also partly involved in the publication service

Ruzica Piskac
Vice Chair of Advisory Team
Yale University, USA

served as editor-in-chief from 2014-2020

Diego Calvanese
Member of Advisory Team
Free University of Bozen/Bolzano, Italy

Laura Hollink
Member of Advisory Team
Centrum Wiskunde & Informatica (CWI), The Netherlands

Friederike Klan
Member of Advisory Team
German Aerospace Center (DLR) Jena, Germany

Jolita Ralyté
Member of Advisory Team
University of Geneva, Switzerland

CEUR-WS.org

Table of Contents

An Intelligent Adaptive DC Voltage Stabilization with a Digital Control Contour

Serhii Tsyrulnyk [1,2], Volodymyr Tromsiuk[1], Yaroslav Borodai [1], Artem Metelytsya [1], and Maxim Nepiyvoda [1]

[1] *Vinnytsia Technical Applied College, Khmelnytske highway, 91/2, Vinnytsia, 21000, Ukraine*
[2] *Vinnytsia National Agrarian University, str. Sonyachna, 3, City, Vinnytsia, 21008, Ukraine*

Abstract

This paper provides an analysis of the operation of the DC voltage stabilization system with a digital control contour, which uses a linear dependence between the opening pulse duration of the power control element and the output voltage deviation from the nominal one. The work presents the structural and functional diagrams of the voltage stabilization system with a digital control contour. The paper conducted simulation modeling of the proposed schemes in the Multism. The design features and technical parameters of linear and pulsed series stabilizers analyzed the principle of step-down linear step-down DC voltage stabilization with pulsed control used as a basis.

DC voltage stabilization system are broadly used in DC microgrids to provide a constant DC voltage for generation and storage components. Changing of load condition affects the quality of voltage in the DC voltage stabilization system. In such condition, an efficient DC voltage stabilization system is required to ensure the proper operation of the converter.

Because of the research, a structural diagram of the DC voltage stabilization system with a digital control circuit was built. Based on the constructed structural diagram, the functional schemes of DC voltage stabilization were developed:

1. DC voltage stabilization system based on a 4-bit current-steering DAC, with reference voltage Vref=Vin;
2. DC voltage stabilization system based on an 8-bit current-steering DAC, with reference voltage Vref=Vin;
3. DC voltage stabilization system is based on a 4-bit current-steering DAC, with a reference voltage of Vref=VCC, and used a Wilson current mirror.

Simulation modeling of the developed circuits showed the expected results of voltage stabilization using a digital control circuit. In particular, a low level of pulsations was observed without using a filter and a soft start when adjusting the output voltage.

Keywords

Digital control contour, ADC, Current-steering DAC, Control element, Digital control device

1. Introduction

Today, DC systems are broadly used in transportation systems, microgrids, different power systems. [1], [2], [3]. The DC microgrids are based on various power electronic devices which add several advantages like low weight and volume, high efficiency and flexibility, as well as isolation, controllability [3], [4], [5]. Switching dynamics of the various DC-DC converter lead the DC microgrids to a nonlinear behavior. Hence, adjusting the output DC voltage is a challenging task [1], [6]. Attaining

COLINS-2023: 7th International Conference on Computational Linguistics and Intelligent Systems, April 20–21, 2023, Kharkiv, Ukraine
EMAIL: sovm@ukr.net (S. Tsyrulnyk); 2013tvd@gmail.com (V. Tromsiuk); bortamugoo@gmail.com (Y. Borodai); artemmetelicha@gmail.com (A. Metelytsya); nepijvoda@gmail.com (M. Nepiyvoda)
ORCID: 0000-0002-5703-9761 (S. Tsyrulnyk); 0000-0001-5022-8159 (V. Tromsiuk); 0000-0002-4071-023X (Y. Borodai); 0000-0001-9131-5320 (A. Metelytsya); 0000-0002-9383-7752 (M. Nepiyvoda)

an appropriate control method for DC-DC converters is an important task to better understand the design aspect of the controller and stability problem [5], [6], [7].

The intelligent adaptive DC voltage stabilization with a digital control contour can be used, for instance, in the IoT (Internet of Things) automatically regulate battery charge. Also, such constant voltage stabilizers can ensure the high energy efficiency of the Low-power Wide-area Network for the IoT [5]. In the IOT network, individual nodes are often implemented as system-on-chip solutions, containing sensors, signal processors, and wireless transceivers. To power the nodes, multiple possible energy sources are available but those sources are typically harvested by inductive or capacitive dc–dc power converters. Compared with impulsive dc–dc proposed DC voltage stabilization with a digital control contour no off-chip inductors and is suitable for monolithic low power energy harvesting applications such as modern IOT smart nodes [1], [5].

The purpose of this work is to design and research a smooth ramp DC voltage stabilization system that can detect and adjust abnormal voltage levels to ensure a sufficiently stable output and control the output voltage through feedback. The DC voltage stabilization system with a digital control circuit is quite intelligent, as it allows you to automatically monitor the change in the output voltage. The reaction to a change in the output voltage changes the parameters of the circuit in such a way as to obtain the most stable voltage value with a minimum error. In addition, the proposed technical solutions make it possible to abandon the use of a voltage amplifier in stabilizer circuits due to the use of a current-steering DAC and a current adder.

It is necessary to solve the following tasks to achieve the goal:

1. Build a DC voltage stabilization with a digital control contour.
2. Build a DC voltage stabilization with a digital control contour using a current-steering DAC using a Wilson current mirror to linearize the voltage/code conversion characteristics.
3. Conduct research and modeling of proposed schemes.
4. Determine the influence of current-steering DAC parameters with current output on the operation of the DC voltage stabilizer.

2. Literature Analysis

When designing such sources, developers prefer pulsed voltage stabilizers, because compared to linear stabilizers, they have undeniable and very significant advantages – these are high efficiency, and, as a result, low heat generation, as well as low weight and small dimensions [1], [8], [9]. However, stabilizers with linear control have a simpler circuit and a lower level of nonlinear distortions, and there is no need to use filters with high selectivity. The linear and pulse combination of voltage stabilization allows us to achieve significantly better results. Using a digital control circuit, they provide significantly better characteristics than other DC voltage stabilization schemes. The digital control circuit allows getting significantly better characteristics than other DC voltage stabilizations. The use of a digital control circuit instead of an analog one makes it possible to eliminate the temperature and time drift of parameters, which is characteristic of analog circuits and is the subject of modern research [3], [10], [11].

Changes in voltage lead to temporary or permanent failure of the load. Due to uncontrolled low or high voltage, the life of computer systems and networks is reduced. Voltage fluctuations occur because of unexpected load changes or problems in the power system. The use of DC voltage stabilization technology with a digital control circuit and power electronic devices in the design of intelligent stabilizers leads to the provision of a stable voltage on the constant power load [11].

It is necessary to provide them with a stable supply voltage for the normal functioning of most computer systems, networks, and other intelligent systems. The main factors that cause voltage fluctuations are power supply voltage fluctuations; change in the frequency of the mains current; load resistance fluctuations and temperature change. Depending on the type of computer systems and networks, the relative change in the supply voltage (output/output voltage) · 100% can vary from 0.005 to 3% or more [12], [13]. Low stability is in which the voltage (current) changes by more than 5%, average - 1...5%, high - 0.1...1%, and precision - less than 0.1% [14]. Intending to tackle climate change, 80 Plus Titanium certification requires server and data storage hardware to deliver 90% power

efficiency levels in 10% load conditions, and 96% efficiencies when dealing with 50% loads," said, Asif Jakwani, senior vice president and general manager, Advanced Power Division, at Onsemi [15].

Classic linear controllers are generally used in DC-DC converter controllers [1]. However, because of the nonlinear feature of the systems, linear control techniques may only guarantee signal stability. However, in large disturbances, they are not effective for load changes. In [1], [4], adaptive backstepping control are used for estimation of uncertain changes in constant power load in a fast dynamic response which resulted in a fast and precise DC voltage tracking under high load changes. The main advantages of backstepping controller are systematic frame for controller design, easy to understand, simple performance, linear parameter inconsistencies, nonconformities, and successful rule out for uncertainty. Adaptive backstepping control is one of the most effective nonlinear synchronous control methods for solving stability and tracking problems [1], [10].

The amount of pulsation of the output voltage determines the electromagnetic compatibility of power sources with the load. Electronic systems based on digital elements require less stable power supply parameters. For example, digital microcircuits require a constant voltage supply with a ripple of no more than 1%. The concept of DC voltage stabilization with a digital control contour allows for eliminating periodic disturbances that multiply the network frequency. Voltage ripples are transferred to higher frequencies, which are determined by an external generator. Such pulsations can be easily smoothed out with an ordinary ceramic capacitor [12], [14], [16].

3. Design of the scheme DC voltage stabilization with a digital control contour with a reference voltage equal to Vin

The organization of the control device DC voltage stabilization in a digital form involves the transition to discrete values, which are limited by the number of discrete values determined by the bit rate of the counter and the current-steering DAC. Therefore, the quality of the output voltage will depend not only on the level of input ripples but also on the bit rate of the counter, the current-steering DAC, and the speed of the ADC.

An example of Figure 1 shows the structural diagram of the DC voltage stabilization system with a digital control contour. The structural diagram consists of a digital control contour and a power-regulating element. In such a system, the control signal of the regulating element is formed in the form of a binary code, which is converted into an analog signal using the current-steering DAC, and an ADC is used to control the output voltage. The value of the DC voltage on the load is estimated by a digital control contour. It compares it with the specified value and modifies the control binary code in such a way that, with the help of the regulating element, the possible deviation of the output voltage is minimized.

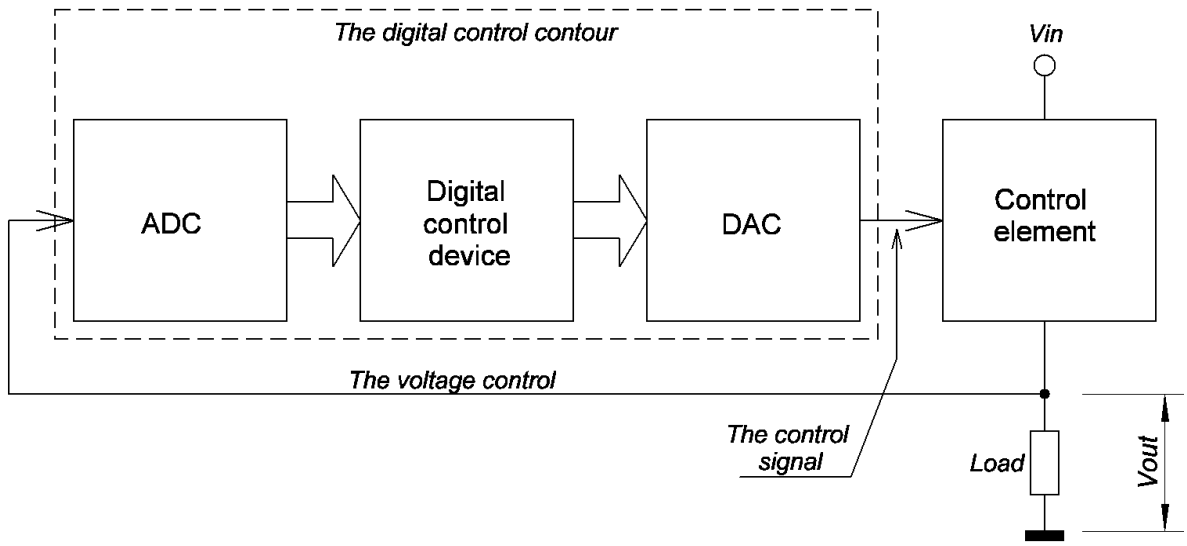

Figure 1: Block diagram of DC voltage stabilization with a digital control contour

The structural diagram in Figure 1 consists of the digital control contour, Control element, and Load. The digital control contour consists of ADC, Digital control device, and the current-steering DAC. The digital control device consists of the comparator and reversing binary counter. In the future, the digital control contour can be replaced by a microcontroller, which will greatly simplify the DC voltage stabilizer system.

The practical implementation of such a DC voltage stabilization system, in the vast majority of cases, involves the use of a DAC based on an R-2R matrix with an output signal in the form of a voltage, the level of which is determined by the formula [17], [18]:

$$Vout = \frac{Vref}{2^n} D \quad (1)$$

where Vref is the value of the reference voltage; n-bit DAC; D is a coefficient determined from 0 to 2^n-1 depending on the input binary code.

Thus, the DAC output signal level does not exceed the reference voltage, which is not critical if the output voltage of the DC voltage stabilization system does not exceed the DAC supply voltage (shown in Figure 2a). Otherwise, the output level of the DAC is not sufficient to control the regulating element and it is necessary to use an additional DC amplifier (shown in Figure 2b).

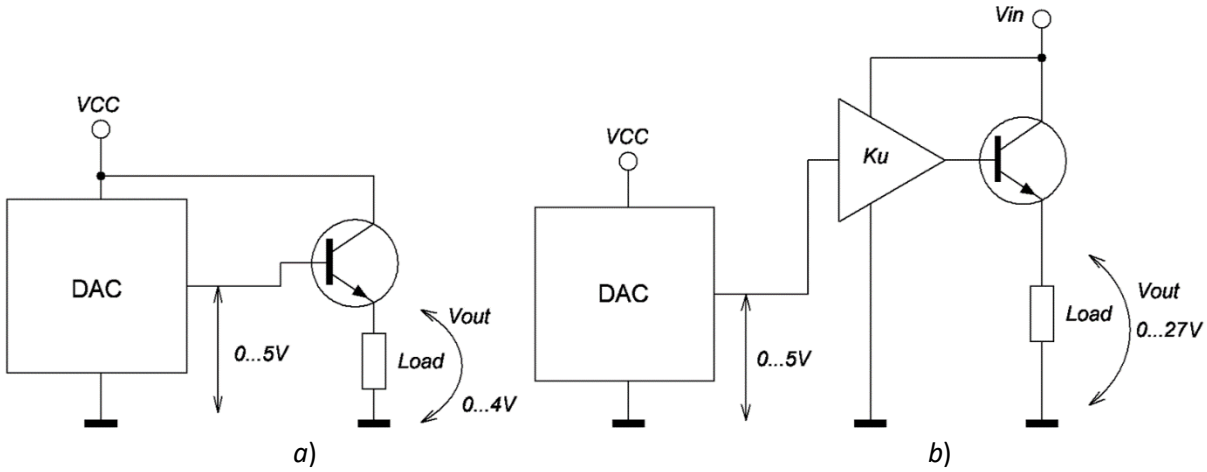

Figure 2: Connecting the DAC to the regulating element: *a*) without an amplifier; *b*) with an amplifier

Such a DC amplifier should have high-temperature stability and the possibility of linear amplification of the input signal with a level of several millivolts, which narrows the possibility of selecting specialized microcircuits and, accordingly, increases their cost. In turn, the disadvantage of the DAC structure with weighted resistors is a wide range of resistance values of resistors that serve to form discharge currents. In addition, to ensure conversion accuracy, resistor ratings must be met with precise accuracy.

3.1. Functional diagram of DC voltage stabilization based on current-steering DAC

The use of the current-steering DAC on binary-weighted resistors as part of a DC voltage stabilization system makes it possible to design stabilizers with an output voltage significantly higher than the supply voltage of the digital part without the use of an amplifier. An example of Figure 3 shows a functional diagram of a possible version of such voltage stabilization with a digital control contour based on current-steering DAC on binary-weighted resistors.

The scheme works as follows. The digital control device forms a control binary code, according to which the corresponding weight resistors are connected and a control signal for the control transistor is formed at the output of the current-steering DAC on binary-weighted resistors. The base current, which is amplified by the transistor by a factor of h_{FE}, flows through the load and creates a corresponding voltage drop on it. Control of the current value of the voltage on the load is carried out through a divider,

which reduces the high output voltage to a level safe for the digital part of the stabilizer, no higher than the level of VCC. The output current of such the current-steering DAC on binary-weighted resistors is described by the formula:

$$\Sigma I = \frac{Vref}{R} x0 + \frac{Vref}{2R} x1 + \frac{Vref}{4R} x2 + \frac{Vref}{8R} x3 + ... + \frac{Vref}{2^n R} xn = \frac{Vref}{2^n R} D \quad (2)$$

where x_n is the value of the binary code, it can be 0 or 1; R is the resistance of the first resistor of the current-steering DAC on binary-weighted resistors.

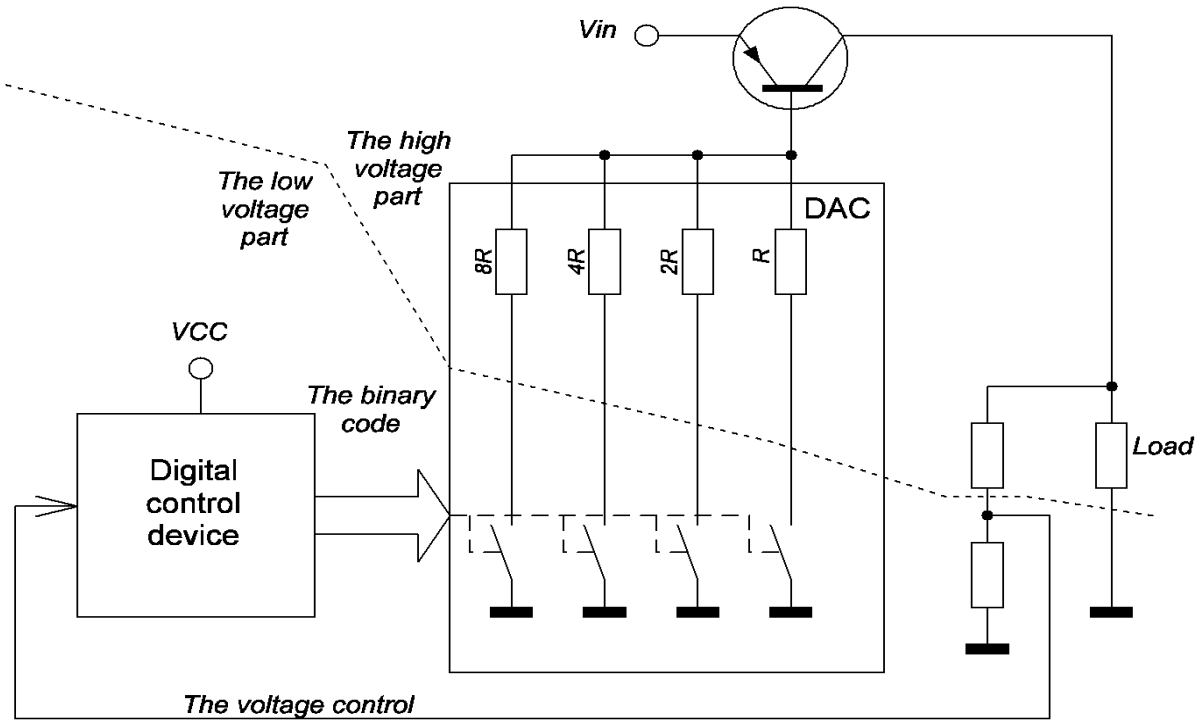

Figure 3: Functional diagram of DC voltage stabilization with a digital control contour

The quantization step is equal to the gradation of the output voltage from the youngest digit:

$$h = Vref \frac{R0}{2^n R} \quad (3)$$

where R0 is the internal resistance of the reference voltage source.

For such a schematic implementation of the current-steering DAC on binary-weighted resistors, the reference voltage is equal to the supply voltage, taking into account the voltage drops at the base-emitter transition of the control element. In this way, it is possible to build DC voltage stabilization with an output voltage that is limited from above only by the opening voltage of the transistor switches. As a key in this case, it is necessary to use a transistor with n-conductivity.

3.1.1. Experimental research DC voltage stabilization based on current-steering DAC scheme in Multisim

Based on the proposed concept of building a DC voltage stabilization system with a digital control contour, a circuit was developed in the Multisim [19] environment, the results of which are shown in Figure 4.

The digital control device is built based on a reversible binary four-bit counter 74193N with a comparator on logic elements. The DAC is implemented on keys based on field-effect transistors with binary weighted resistors. A single-bit ADC is built on an operational amplifier and a zener diode to limit the output level to the value of a logical unit of digital logic. The regulating element is built based on a bipolar transistor of the p-n-p structure. A typical HEX indicator is used for visual control of the

control binary code from the output of the digital control device. Regulation of the output signal is ensured by changing the threshold level at the input of the operational amplifier by a potentiometer, which is powered by a source of a stabilized reference voltage.

Figure 5 shows the oscillogram of the output voltage of the DC voltage stabilization scheme with a digital control contour, from which it can be seen that the voltage on the load after turning on the power gradually (without emissions) increases from zero to a certain value and then follows it with a certain level of pulsation. In essence, the digital control contour provides an adaptive change in the output DC voltage depending on the load change.

The DC voltage on the load varies in a relatively narrow range. This principle of setting the voltage on the load shows the features of linear and impulse control. This principle allows you to smooth out pulsations with an ordinary ceramic capacitor of small capacity. Reducing the requirements for selecting a filter allows you to increase the efficiency and reduce the dimensions of the DC voltage stabilizer system.

If you limit the supply voltage of the Vin DC voltage stabilization system to 30V, it becomes possible to use 7406N buffer elements (inverters with an open collector) as transistor switches, with a maximum operating voltage of 30V and an output current of 40mA [20]. When the input voltage level of the DC stabilizer with a digital control contour exceeds 30V, power elements that operate at higher voltages must be used.

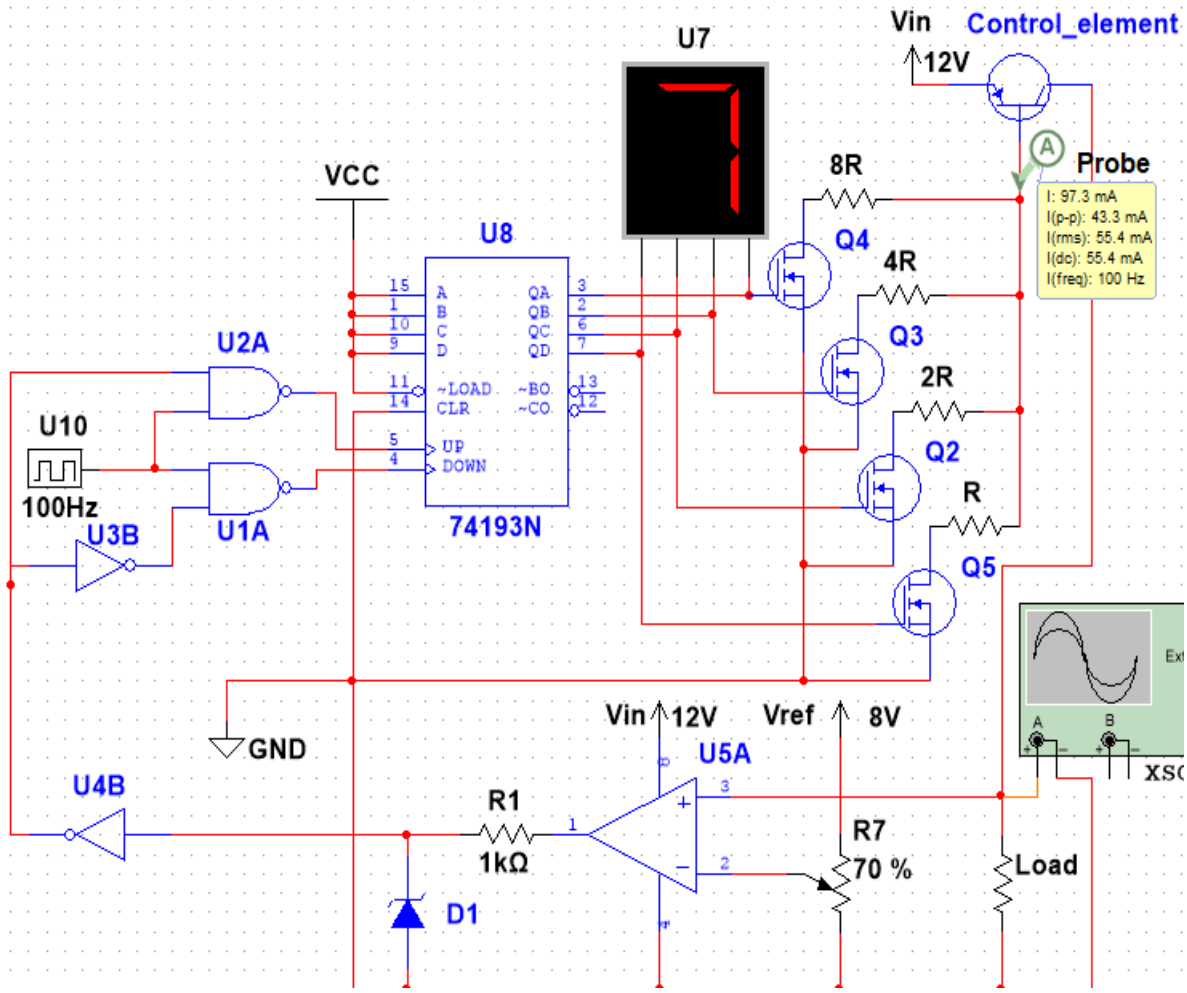

Figure 4: DC voltage stabilization scheme with a digital control contour based on a reversing counter

The results of the study of a modified DC voltage stabilization scheme with a digital control circuit using two 74193N reversing counters and eight 7406N buffer elements are shown in Figure 6. That is, an 8th divided current-steering DAC on binary-weighted resistors is formed in this way, which increases the number of possible counts to 256.

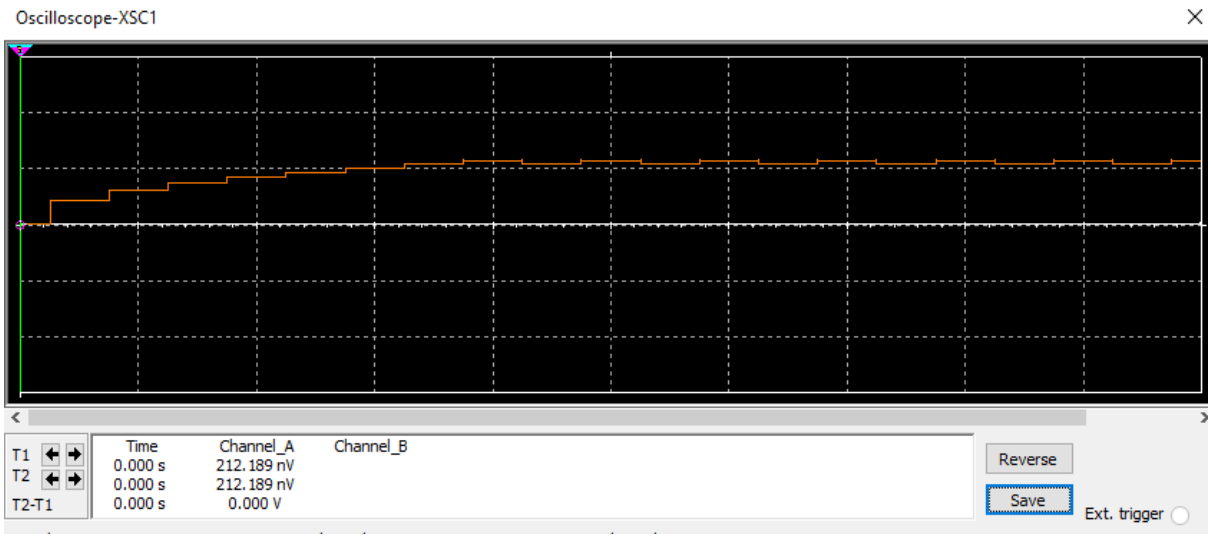

Figure 5: Oscillogram of DC voltage scheme with a digital control contour based on a reversing counter on the load

The scheme shown in Figure 6 works in the same way as the scheme shown in Figure 4, with the difference that in the latter scheme, there are 256 steps of changing the output voltage, and in the first scheme there are only 16 of them.

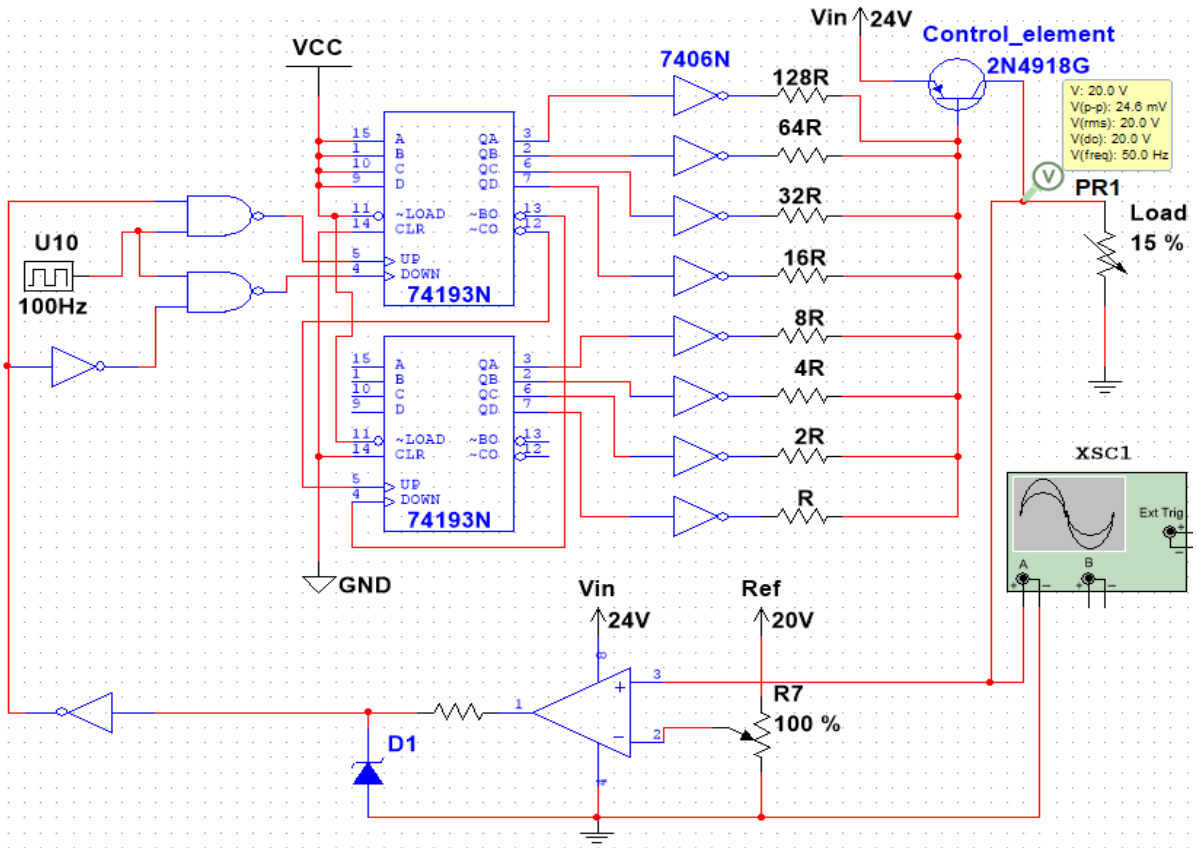

Figure 6: A modified DC voltage stabilization scheme with a digital control contour based on two reversing counters

The oscillogram of the operation of the modified voltage stabilization system for a fixed load of 15Ω at different values of the output voltage: 20V, 16V, 12V, 4V, and 8V is shown in Figure 7. Each shelf corresponds to the stabilized level of the output voltage on the load.

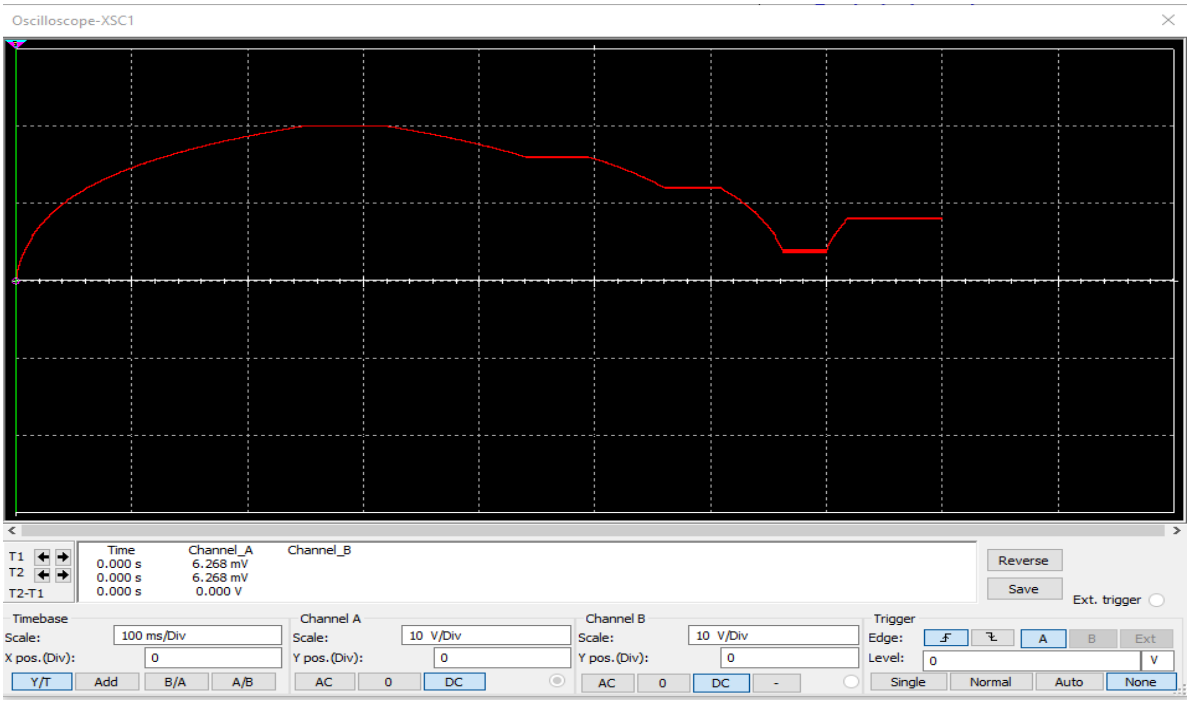

Figure 7: The oscillogram of the output voltage of the modified DC voltage stabilization scheme is built based on an 8-bit current-steering DAC on binary-weighted resistors

The analysis of the oscillogram indicates a clear nonlinearity of the control code-output voltage dependence, which is caused by the dependence of the base current gain of the 2N4918G control element on the collector current, which is shown in Figure 8 [21]. As can be seen from the dependence, when the collector current increases from 15mA to 1500mA, the transmission coefficient h_{FE} decreases from 150 to 18. This dependence affects the operation of the circuits shown in Figures 4 and 6.

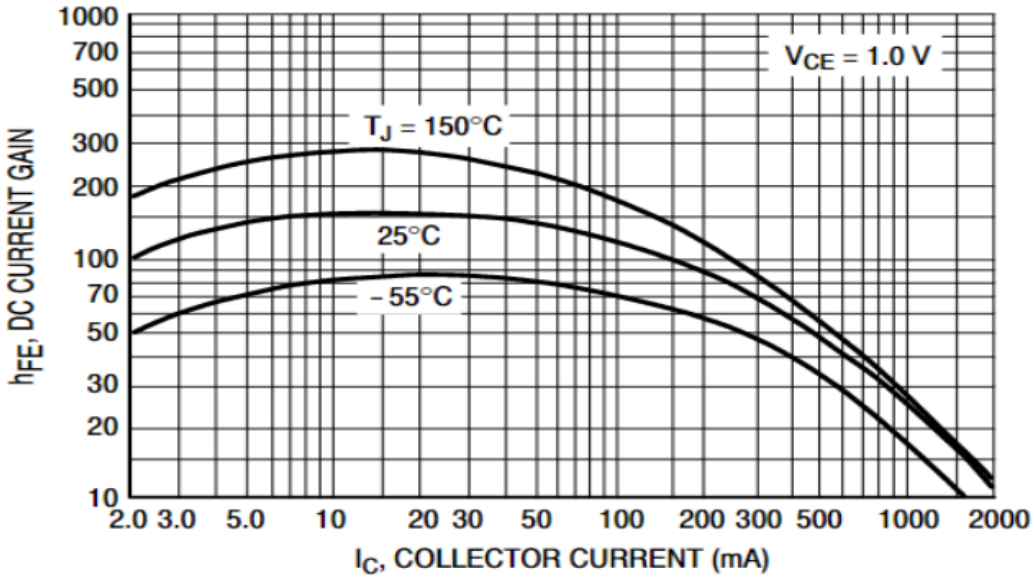

Figure 8: Current Gain for the 2N4918G transistor

The implementation of the functional circuit of the DC voltage stabilization based on the current-output DAC shown in Figures 4 and 6 uses the supply voltage Vin, taking into account the voltage drops at the base-emitter junction of the regulating transistor, as a reference voltage. Thus, with fluctuations (pulsations) of the supply voltage Vin and a fixed code at the output of the digital control device, the output current of the DAC is modulated, which is a control signal for the regulating transistor, which manifests itself in the form of additional voltage ripples on the load.

3.1.2. Experimental research of the influence of input voltage ripples on the load voltage

The results of the study of the influence of the supply voltage fluctuation on the output voltage ripple are shown in Figure 9. The conditions of the research: supply voltage Vin=24V, the pulsation shape is sinusoidal, the amplitude of the pulsations is 2.8V, the frequency is 50Hz, the frequency of the clock generator is 1000Hz and 100kHz (the ratio of the frequency of the pulsations on the load to the frequency of pulsations of the supply voltage 10:1 and 1000:1), the output voltage of the stabilizer is 12V. The oscillogram of the load voltage at different ratios of the clock frequency of the generator to the pulsation frequency of the supply voltage is shown in Figure 10.

The oscillogram of the load voltage at different ratios of the clock frequency of the generator to the pulsation frequency of the supply voltage is shown in Figure 10-12.

The analysis of the results of the study of the effect of power supply voltage ripple on the output voltage of the stabilizer at different frequencies of the clock generator shows that the level of ripples under ideal conditions (Vin=const) is 332 mV (Figure 10). When the supply voltage fluctuates within ± 11.7% and the ratio between the oscillation frequency (Fu10) and the pulsation frequency (Fin) of the supply voltage is 10:1, the amplitude of the pulsation on the load is Vload=1.24V (Figure 11). When the ratio of the oscillation frequency (Fu10) of the load voltage to the fluctuations frequency of the supply voltage is 100:1, the pulsation amplitude is 945 mV (Figure 12). Accordingly, the growth of ripples in relation to ideal conditions occurs by 3.7 times (1.24V/332mV) at a frequency ratio of 10:1 and by 2.8 times (945mV/332mV) at a frequency ratio of 100:1.

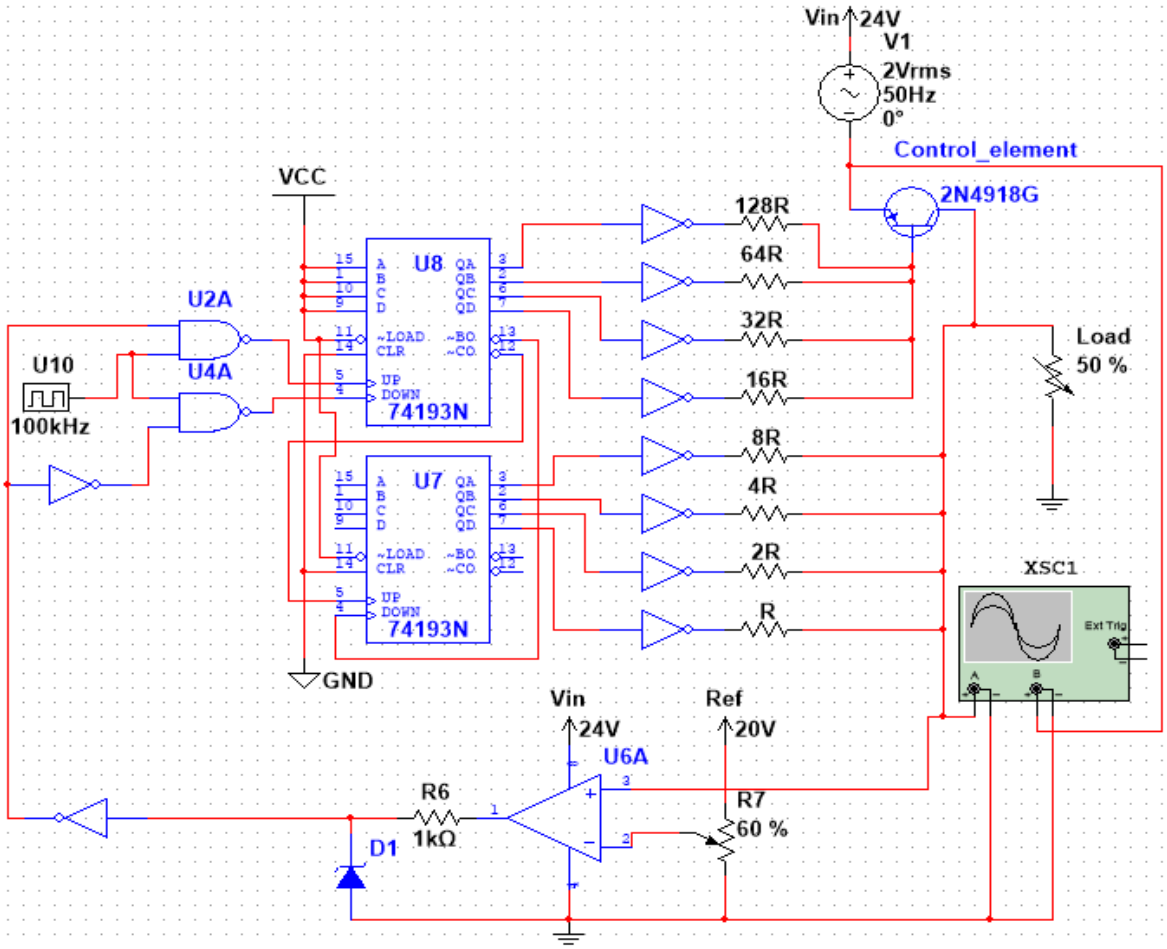

Figure 9: The results of the research of the influence of input voltage ripples on the load voltage

Therefore, the use of a DAC with a surge output, which is built according to the functional scheme shown in Figure 3, leads to a significant additional increase in the level of output voltage ripples relative to what is observed under ideal conditions.

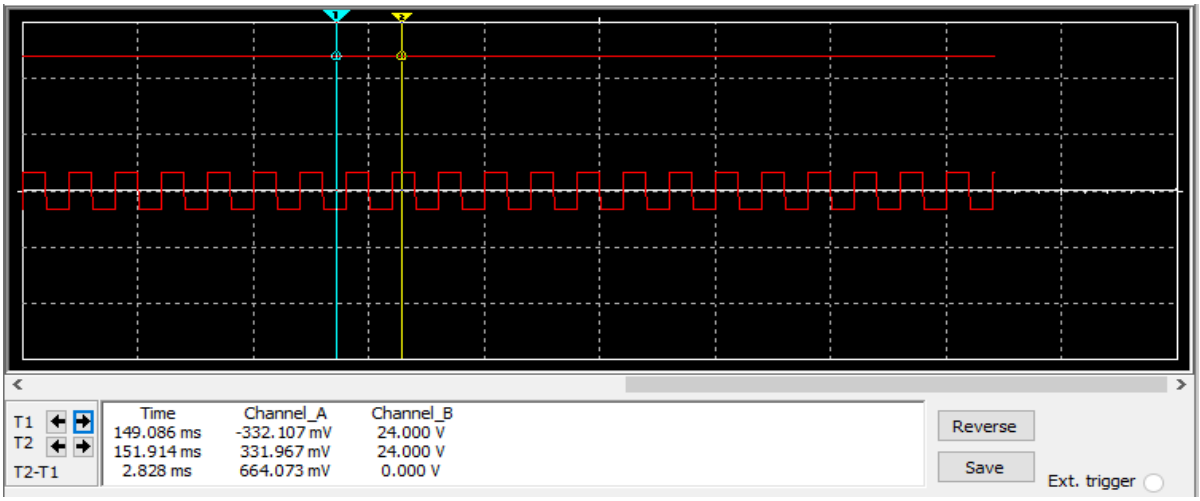

Figure 10: The results of the research on the influence of input voltage ripples on the load voltage (Vin without ripples; Vload= 332 mV; Fin:Fu10 =1:10)

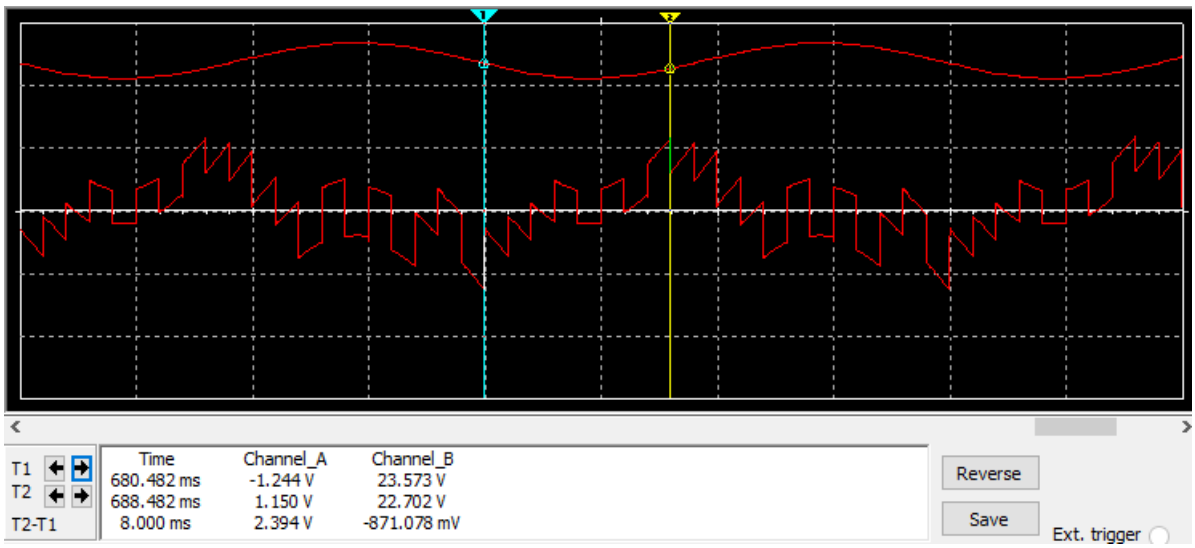

Figure 11: The results of the study of the influence of input voltage ripples on the load voltage (Vin with 2,8V ripples; Vload= 1,24 V; Fin:Fu10=1:10)

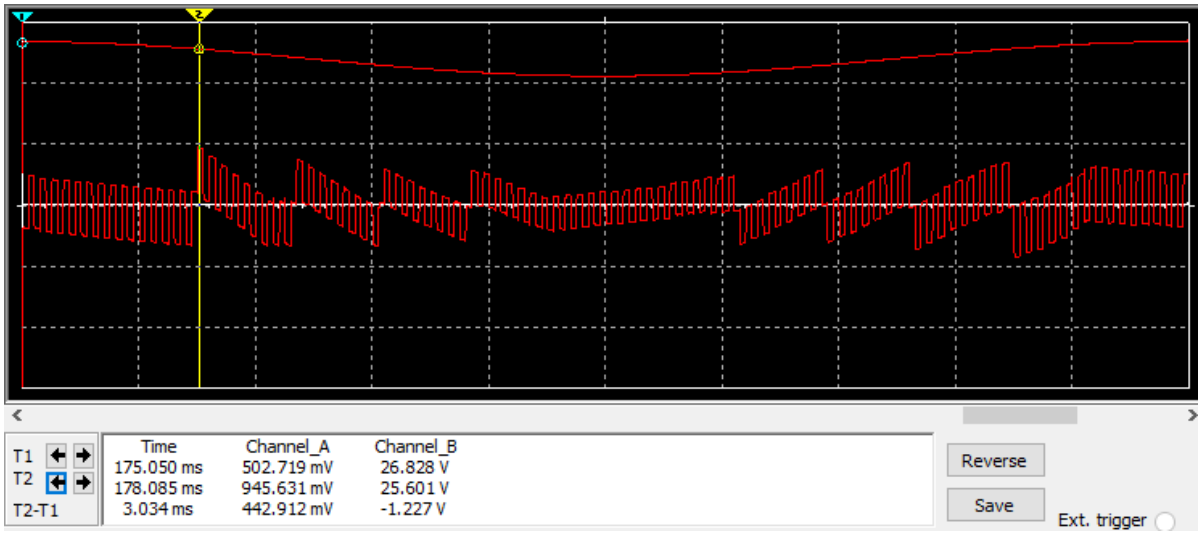

Figure 12: The results of the study of the influence of input voltage ripples on the load voltage (Vin with 2,8V ripples; Vload= 945 mV; Fin:Fu10=1:100)

3.2. Design of the functional diagram DC voltage stabilization with a digital control contour with a reference voltage equal to VCC

It is possible to get rid of the influence of supply voltage fluctuations when building a DAC with a current output with the simultaneous possibility of increasing the output voltage of the stabilization system above the supply voltage of the digital part (UL>VCC) by applying the schematic solutions shown in Figure 13.

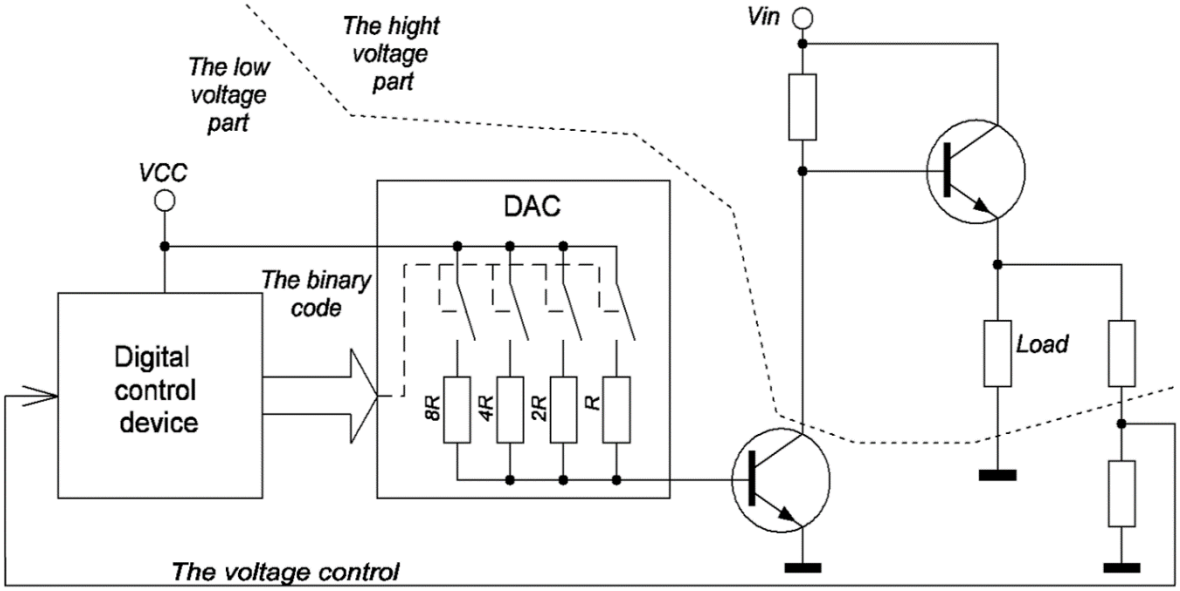

Figure 13: Functional diagram of voltage stabilization based on current-steering DAC and stabilized reference voltage

In the given scheme, the digital control device forms a binary code, according to which the corresponding weighting resistors are connected and a control signal (base current) is formed at the output of the DAC, which is amplified by the transistor VT1 and causes a voltage drop on the collector resistor. Transistor VT2 is a current amplifier that forms the output voltage on the load. Control of the current value of the voltage on the load is carried out through a divider, which reduces the high output voltage to a safe level for the digital part of the stabilizer (ADC is conventionally not shown). The output current of the DAC shown in the figure is described by the formula (2).

3.2.1. Experimental research DC voltage stabilization with a digital control contour with a reference voltage equal to VCC

Based on the proposed functional scheme (Figure 13) of stabilization with a digital control circuit, a device scheme was developed, the results of which are shown in Figure 14.

The digital control device is made on two reversible binary four-bit counters 74193N with a comparator. A single-bit ADC is built on an operational amplifier and a zener diode to limit the output level to the value of a logical unit of digital logic. The eight-bit current-steering DAC is implemented on weight resistors with switches on p-channel field-effect transistors. The regulating element is a bipolar compound transistor according to the Darlington scheme of the n-p-n structure. In order to linearize the dependence of the control code - voltage on the load, a Wilson current mirror [22], [23], [24] is applied on transistors T1, T2, T3. The load voltage (Vload) is adjusted by a potentiometer by changing the threshold level at the input of a one-bit ADC (operational amplifier).

The oscillogram of the result of the research scheme (Figure 14) 15Ω at different values of the load voltage: 20V, 16V, 12V, 8V, 4V, and 3V is shown in Figure 15. Each value of the DC output voltage

is highlighted by a step, and the transition by a linear gradient. It can be seen from the figure 15 that the output voltage changes smoothly and linearly.

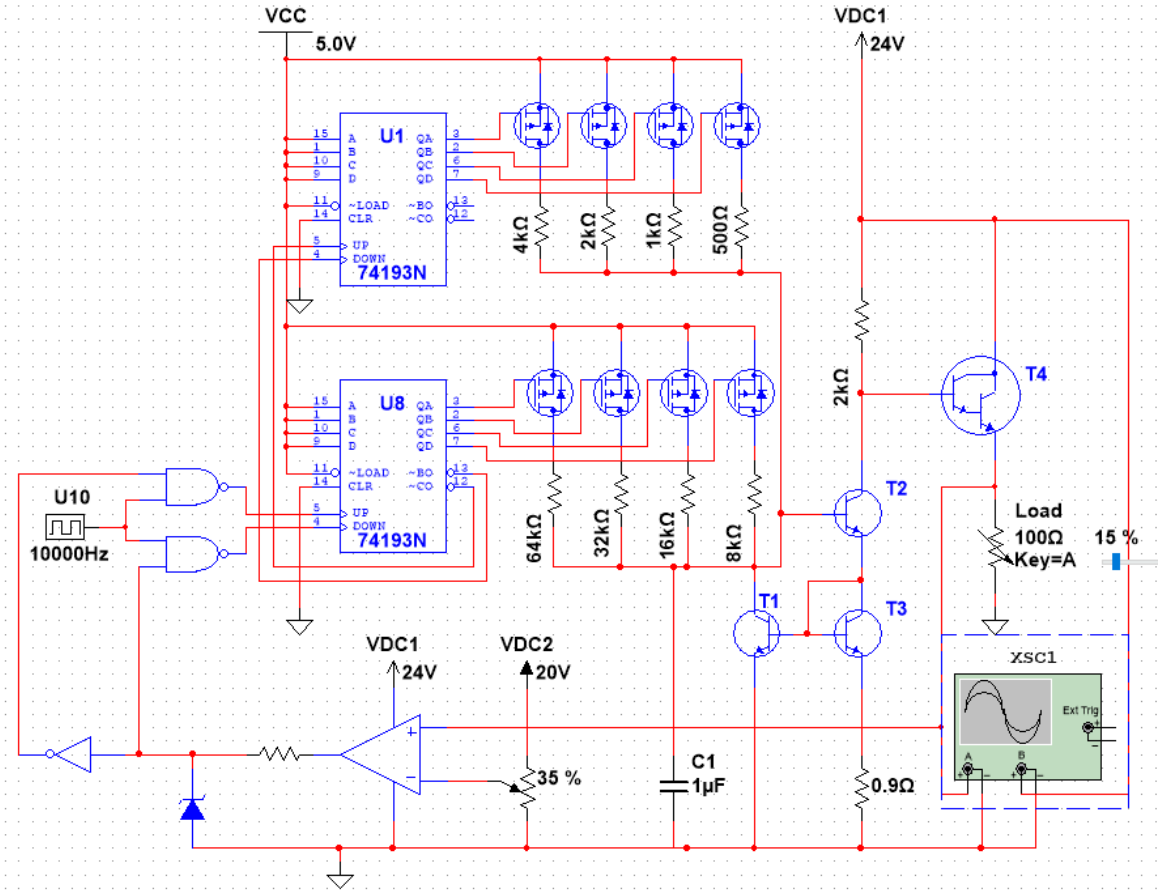

Figure 14: DC voltage stabilization circuit with digital control contour based on current-steering DAC and stabilized reference voltage

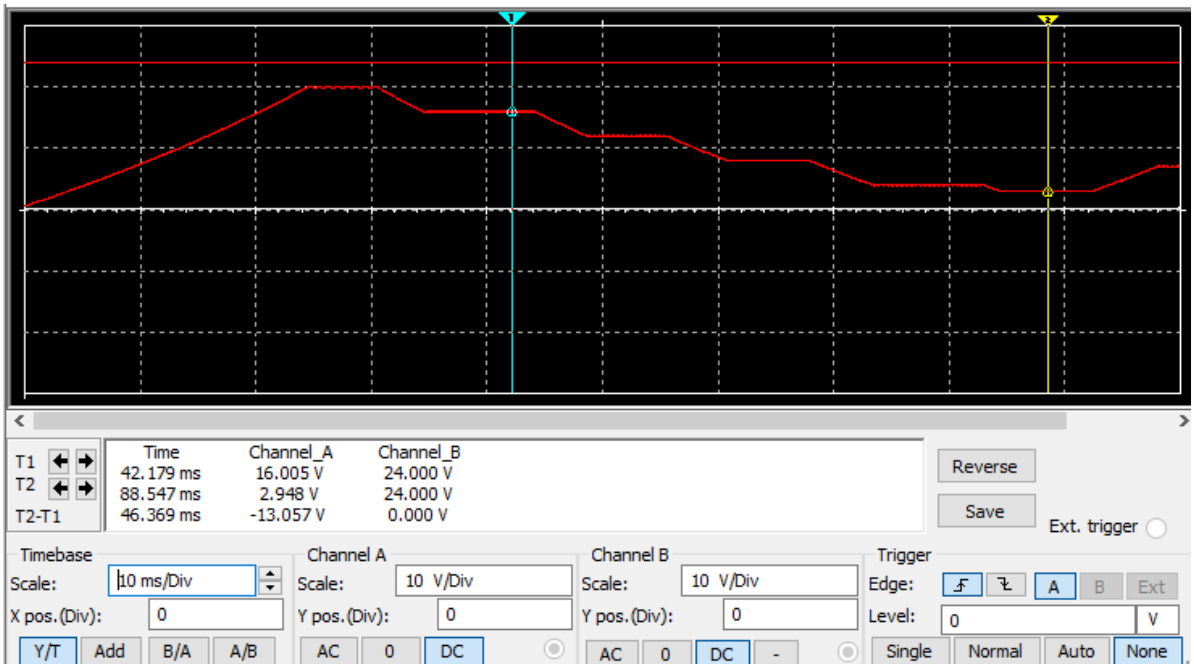

Figure 15: Oscillogram of the research scheme at different set voltage levels: 20V, 16V, 12V, 8V, 4V, and 3V

The oscillogram of voltage pulsations on the load for the set voltage levels of: 20V, 16V, 12V, 8V, 4V, and 3V is shown in Figure 16.

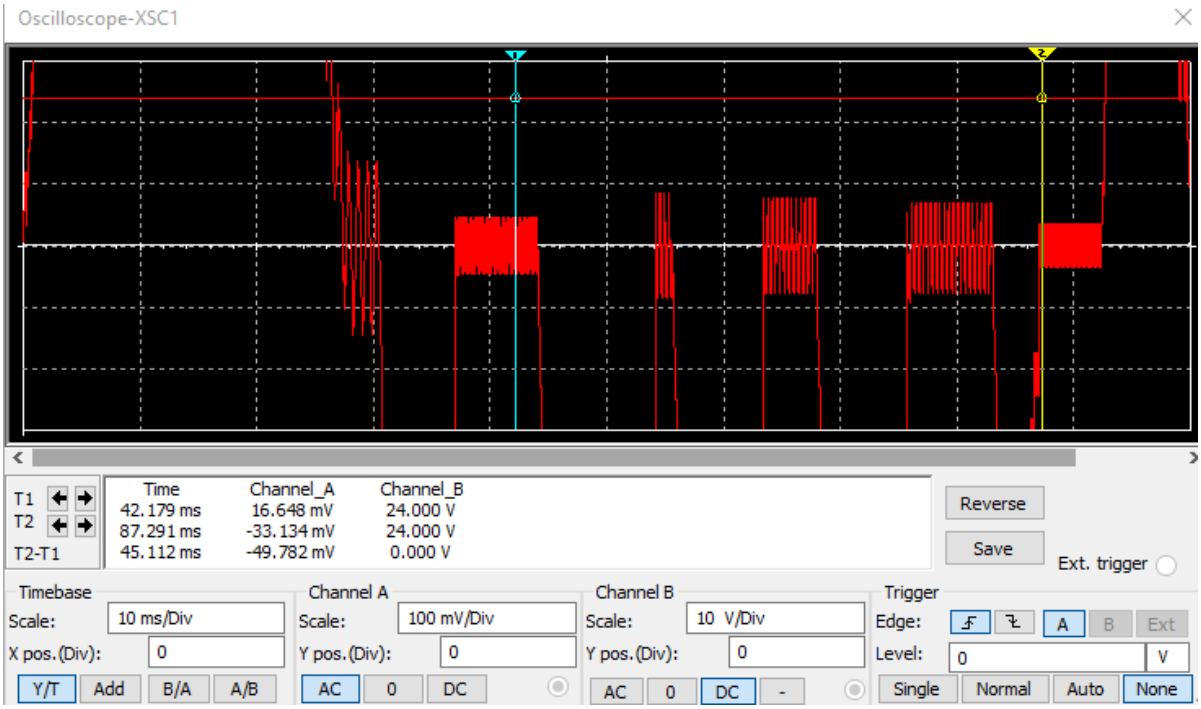

Figure 16: Voltage ripples on the load at different set voltage levels: 20V, 16V, 12V, 8V, 4V, and 3V

The results of the study of scheme 14 show that the level of voltage ripples on the load is lower than that of scheme 9.

4. Conclusions

In the paper, a research of DC voltage stabilization with a digital control contour was conducted, based on the results of which the following conclusions can be drawn:

1. It has been previously established that DC voltage stabilization with a digital control contour based on a voltage DAC contains a DC amplifier that must have high-temperature stability and the ability to amplify a signal starting from a few millivolts relative to zero, which narrows the possibility of selecting microcircuits and increases their value.
2. Two variants of schematic solutions with regulating transistors of the p-n-p type (Figures 3, 4, 6, 9) and n-p-n type (Figures 13, 14) based on a current-steering DAC on binary-weighted resistors are proposed, which makes it possible to design stabilizers with a voltage on the load Vload, which can significantly exceed the recovery voltage of the digital circuit VCC without the use of an additional DC amplifier.
3. To simplify the demonstration of the principle of operation of the proposed circuit solutions for both types of circuits, the ADC is implemented by a single-bit operational amplifier, and the digital control device made of available reversible counters and digital logic elements.
4. The research circuits form the voltage on the load in the form of the sum of the constant level and the pulsating component, which has an amplitude corresponding to the quantization level of the junior circuit of the current-steering DAC, and a frequency two times lower than the frequency of the clock generator of the digital control contour.
5. Circuits on one p-n-p type transistor (Figures 3, 4, 6, 9) have a non-linear relationship between the control code and the load voltage, which leads to an uneven quantization step by level and a conditional dependence of the gain of the control transistor on the magnitude of the collector current.
6. Stabilization of direct current voltage built according to the functional scheme shown in Figure 3 can suppress the passage of pulsation from the supply voltage circuit Vin to the load circuit. The

effectiveness of such suppression is correlated with the ratio of the frequency of the clock generator to the pulsation frequency of the supply voltage Vin, which gives the direction of finding the optimal value of the frequency of the clock generator of the digital control contour.

7. DC voltage stabilization built according to the functional scheme shown in Figure 13 has a stabilized reference voltage. At the same time, the use of Wilson's current mirror as part of the current-steering DAC linearizes the dependence of the control code - the load voltage, which equalizes the quantization step at low and high set levels of the load voltage.

8. Proposed versions of the current DAC with binary-weighted resistors require preliminary selection of the resistances of the resistors and have a limitation on the number of effectively working discharges, which can be overcome by using a microcontroller as a digital control device.

9. The proposed principles of the construction of DC voltage stabilization with a digital control contour can design power supply devices for computer systems and networks.

5. References

[1] Sorouri, H., Sedighizadeh, M., Oshnoei, A., & Khezri, R. An intelligent adaptive control of DC-DC power buck converters. International Journal of Electrical Power & Energy Systems, 141, 2022, 108099. DOI: 10.1016/j.ijepes.2021.108099.

[2] Elsisi, M., Tran, M. Q., Hasanien, H. M., Turky, R. A., Albalawi, F., & Ghoneim, S. S. Robust model predictive control paradigm for automatic voltage regulators against uncertainty based on optimization algorithms. Mathematics, vol. 9, no. 22, 2021, pp. 2885. DOI: 10.3390/math9222885.

[3] Amiri, H., Markadeh, G. A., Dehkordi, N. M., & Blaabjerg, F. Fully decentralized robust backstepping voltage control of photovoltaic systems for DC islanded microgrids based on disturbance observer method. ISA transactions, vol. 101, 2020, pp. 471-481. DOI: 10.1016/j.isatra.2020.05.015.

[4] Olival, P., Madureira, A., & Matos, M. Advanced voltage control for smart microgrids using distributed energy resources. Electric Power Systems Research, vol. 146, 2017, pp. 132-140. DOI: 10.1016/j.epsr.2017.02.014.

[5] Ahmed Hasnain, et all, Designing an IoT based stabilizer for home appliances. 2021. PhD Thesis. Brac University.

[6] Zhou, Y., Zhang, J., Yang, X., & Ling, Y. Optimization of PID controller based on water wave optimization for an automatic voltage regulator system. Information Technology and Control, 48(1), (2019) 160-171.

[7] Ali, M., Anwar, N., Zahra, S. T., Hayat, A., Zaffar, S., & Iqbal, S. Triac based automatic voltage stabilizer. University of Wah Journal of Science and Technology (UWJST), 3, (2019) 23-28.

[8] Devarapalli, R., Bhattacharyya, B., & Sinha, N. K. An intelligent EGWO-SCA-CS algorithm for PSS parameter tuning under system uncertainties. International Journal of Intelligent Systems, 35(10), (2020) 1520-1569.

[9] Zuo, S., Altun, T., Lewis, F. L., & Davoudi, A. Distributed resilient secondary control of DC microgrids against unbounded attacks. IEEE Transactions on Smart Grid, 11(5), (2020) 3850-3859.

[10] Fernandez-Serantes, L. A., Casteleiro-Roca, J. L., Berger, H., & Calvo-Rolle, J. L. Hybrid intelligent system for a synchronous rectifier converter control and soft switching ensurement. Engineering Science and Technology, an International Journal, 35, (2022) doi.org/10.1016/j.jestch.2022.101189.

[11] Holovatyy, A., Łukaszewicz, A., Teslyuk, V., & Ripak, N. Development of AC Voltage Stabilizer with Microcontroller-Based Control System. In 2022 IEEE 17th International Conference on Computer Sciences and Information Technologies of CSIT, IEEE, Lviv, Ukraine, 2022, pp. 527-530. DOI: 10.1109/CSIT56902.2022.10000461.

[12] Fallahzadeh-Abarghouei, H., Nayeripour, M., Hasanvand, S., & Waffenschmidt, E. Online hierarchical and distributed method for voltage control in distribution smart grids. IET Generation, Transmission & Distribution, 11(5), (2017) 1223-1232. doi.org/10.1049/iet-gtd.2016.1096.

[13] Wang, X., Loh, P. C., & Blaabjerg, F. Stability analysis and controller synthesis for single-loop voltage-controlled VSIs. IEEE Transactions on Power Electronics, 32(9), (2017) 7394-7404. DOI: 10.1109/TPEL.2016.2632065.
[14] D. K. Singh, J. Singh and R. R. Ravela, Design and Performance Study of Cost-Effective Smart Servo Controlled Automatic Voltage Stabilizer. 2020 International Conference on Electrical and Electronics Engineering of ICE3, Gorakhpur, India, 2020, pp. 211-215, doi: 10.1109/ICE348803.2020.9122815.
[15] Onsemi Launches High-Performance, Low Power-Loss SUPERFET V Family of MOSFETs for Server and Telecom Applications, 2021. URL: https://www.onsemi.com/company/news-media/press-announcements/en/onsemi-launches-high-performance-low-power-loss-superfet-v-family-of-mosfets-for-server-and-telecom-applications.
[16] Tsyrulnyk, S., Tromsyuk, V., Vernygora, V., Borodai, Y. Simulation of logic elements in reversemode for building neural networks. Computational Linguistics and Intelligent Systems, Proceedins of the 5th International Conference of COLINS, Lviv, Ukraine, (2021), p. 1754-1769.
[17] Lee, W. J., & Sul, S. K. DC-link voltage stabilization for reduced DC-link capacitor inverter. IEEE Transactions on industry applications, 50(1), (2013) 404-414. DOI: 10.1109/TIA.2013.2268733.
[18] Patel, Jayesh, and Amisha Naik. A Low Voltage High-Speed Segmented Current Steering DAC for Neural Stimulation Application. International Journal of Recent Technology and Engineering, 8(5), (2020) 4270-4274.
[19] Discover Electronics. URL: https://www.multisim.com/.
[20] SN7406N Datasheet (PDF) - Texas Instruments, 2001. URL: https: //pdf1.alldatasheet.com/datasheet-pdf/view/27354/TI/SN7406N.html.
[21] 2N4918G Datasheet (PDF) - ON Semiconductor, 2004. URL: https: //pdf1.alldatasheet.com/datasheet-pdf/view/549965/ONSEMI/2N4918G.html.
[22] Mechkov, C. Equalizing the currents in Wilson current mirror. In International Scientific Conference Computer Science, Sofia, Bulgaria, 2008, pp. 248-252.
[23] Luo, Shien-Chun, Ching-Ji Huang, and Yuan-Hua Chu. A wide-range level shifter using a modified Wilson current mirror hybrid buffer. IEEE Transactions on Circuits and Systems I: Regular Papers 61(6), (2014) 1656-1665. DOI: 10.1109/TCSI.2013.2295015.
[24] Zhai, L., Hu, G., Lv, M., Zhang, T., & Hou, R. Comparison of two design methods of EMI filter for high voltage power supply in DC-DC converter of electric vehicle. IEEE Access, 8, (2020) 66564-66577. DOI: 10.1109/ACCESS.2020.2985528.